

PCB@
PCB 33A LA-J891P REV1 M/B 4
DAB00071010

LOGO@
ROYALTY HDMI W/LOGO+HDCP
RO0000003HM

X4E@
SMT EMC EG0 G1 G1R FOR EE AJ891 FH51M
X4EALYBOL01

X4EFP@
PCBA EMC EG0 G1 G1R W/FP AJ891 FH57M
X4EALYBOL51

Compal Confidential

MB Schematic Document

FH52M
LA-J891P

Rev:1A

2020.03.02

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mDP - JDP1
- VGA Port E
P. 39

HDMI - JHDMI1
- VGA Port C
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VBIOS ROM
- SOP8
- Size : 1M
P. 29

N18E-G0/G1/G1R
- MAX-Q
- GDDR6 6G/8G
P. 25-37

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- CPU eDP
P. 38

**CoffeeLake H Processor
BGA1440 (42X28)
(CFL-H & CML-H_ 8+2)**
P. 6-13

Memory BUS

Interleaved (DDR4 2400/2666)

- DDR4 So-DIMM 260 pin
- Channel A
- BANK 0,1,2,3
- Address : 0XA0/1 P. 23

- DDR4 So-DIMM 260 pin
- Channel B
- BANK 4,5,6,7
- Address : 0XA3/4 P. 24

PEG x16
8GT/s

X4 DMI

**Cannonlake PCH - H
FCBGA874 (25X24)**
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**CFL-H : HM370
CML-H : HM470**

SPI ROM 16M
- SOP8
- Size : 16M
P. 16

SPI

LPC/eSPI BUS

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- NPCT750
P. 66

EC KB9022
P. 58

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- KSI/KSO
- W/BL or 4 Zone RGB
P. 63

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- I2C
- KC3810 P. 59

Fan Control*2
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- PCH I2C0
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- EC PS2
- PCH I2C1 P. 63

HD Audio

I2C

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- USB3.1 Port3&4
- RTS5441E
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- GEN2
- On M/B
- Port 1
- W/USB Charger (SLGC55544)
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- GEN2
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- GEN2
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- Port 14
- E2600
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- PCIE 2.0 5GT/s
- PCIE Port 21-24
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- PCIE Port 9-12
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- Port 13 (SATA 0B)
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- PCH I2C2
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Finger print
- USB2 Port 8
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DDC Camera
- Port 5
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WIFI - JNGFF1
- PCIE1.0 2.5GT/s
- PCIE Port 15
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HDA Codec
- ALC295
P. 56

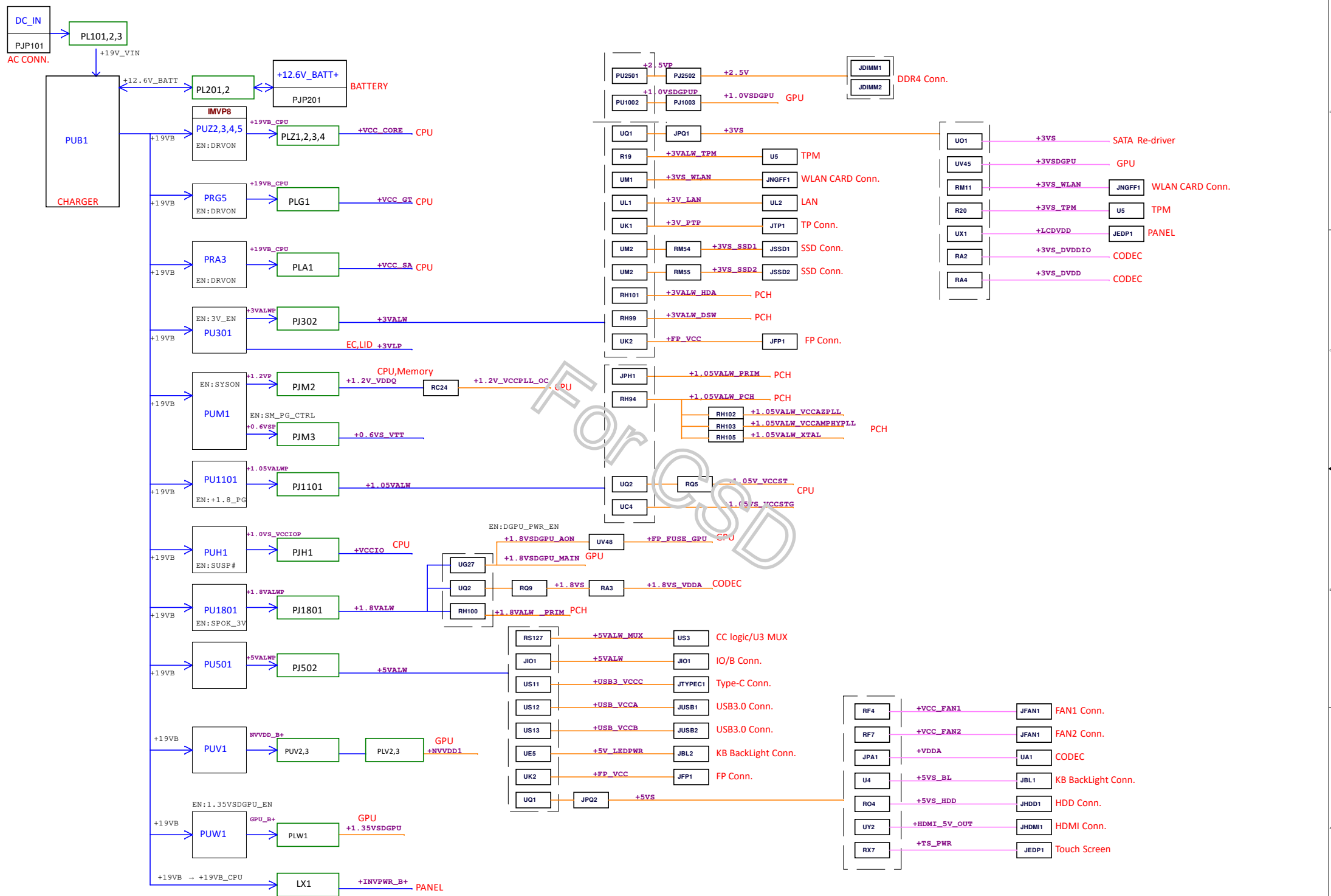
Audio Jack
- On IO/B
P. 56

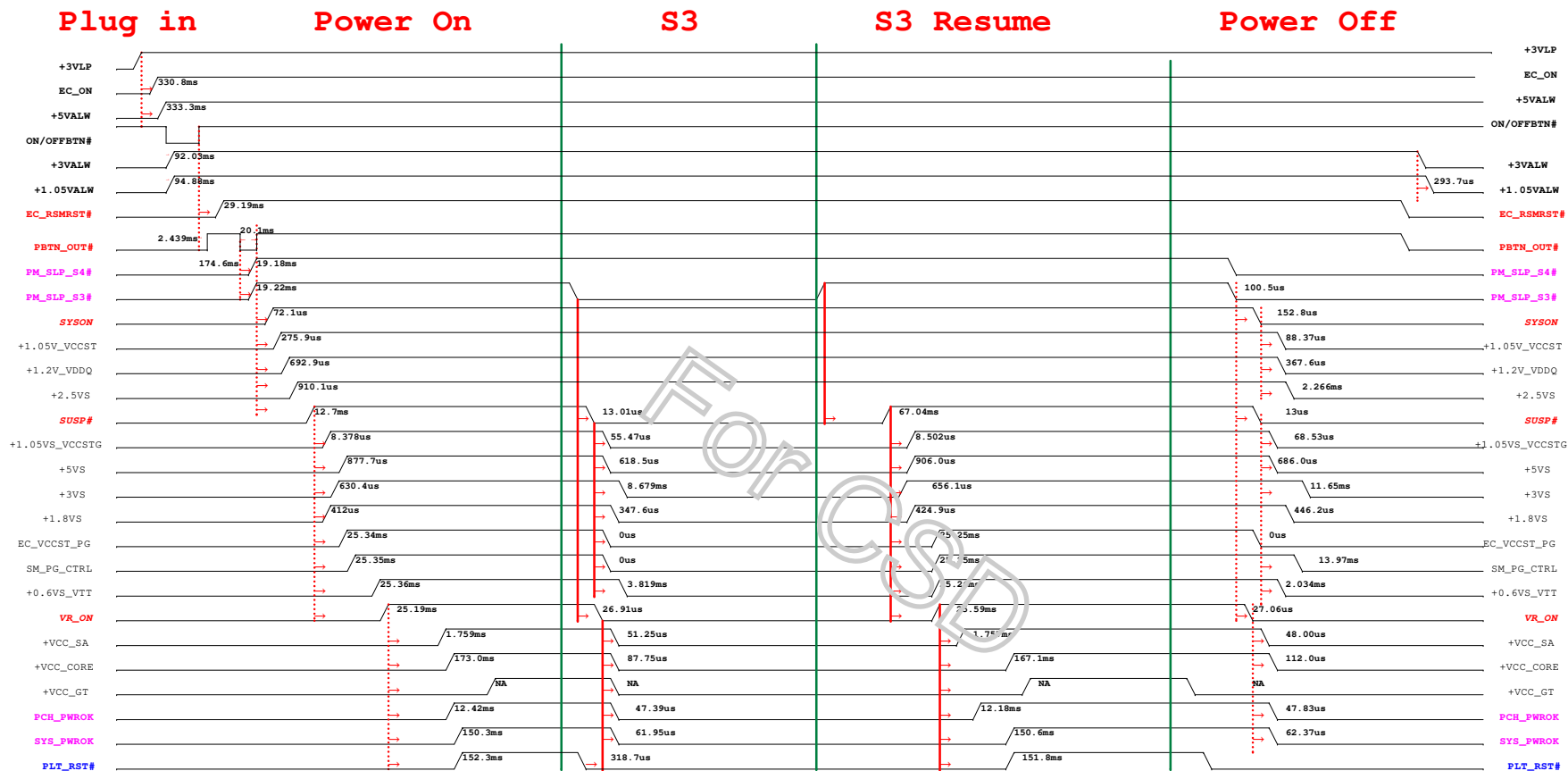
Int. DMIC
- On CCD Module
P. 56

Int. Speaker
- ON IO/B > L
- ON M/B > R
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Sub Board	
IO/B (JIO1/JIO2)	P. 73
HS/B (JHS1)	P. 66
TURBO/B (JTURBO1)	P. 77
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Power On/Of f CKT	
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HW Circuit DC/DC	
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Power Circuit DC/DC	
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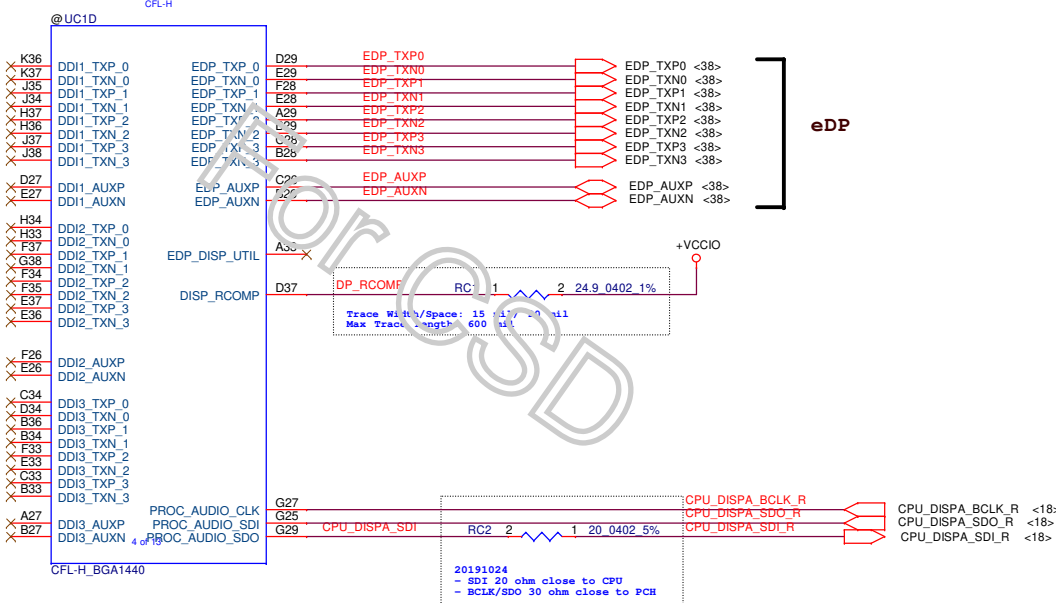


Coffee Lake-H
- Re-fresh R0 stepping

UC1
S QS@
S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00
UH1
S PCHQS@
S IC FH51M370 QNYF B0 BGA 874P PCH-
SA0000BPF10

Comet Lake-H

UC1
S CMLI5@
S IC CL8070104398806 QTJ1 R0 2.1G 1440 S
SA0000D3H10
UC1
S CMLI7@
S IC CL8070104398908 QTJ2 R0 2.4G 1440 S
SA0000D3N10
UC1
S CMLI9@
S IC CL8070104399007 QTJ0 R0 2.8G S
SA0000D3G10
UH1
S CMLPCH@
S IC FH55SKU_MBL QS64 A0 FCBGA 874P S
SA0000D3F10



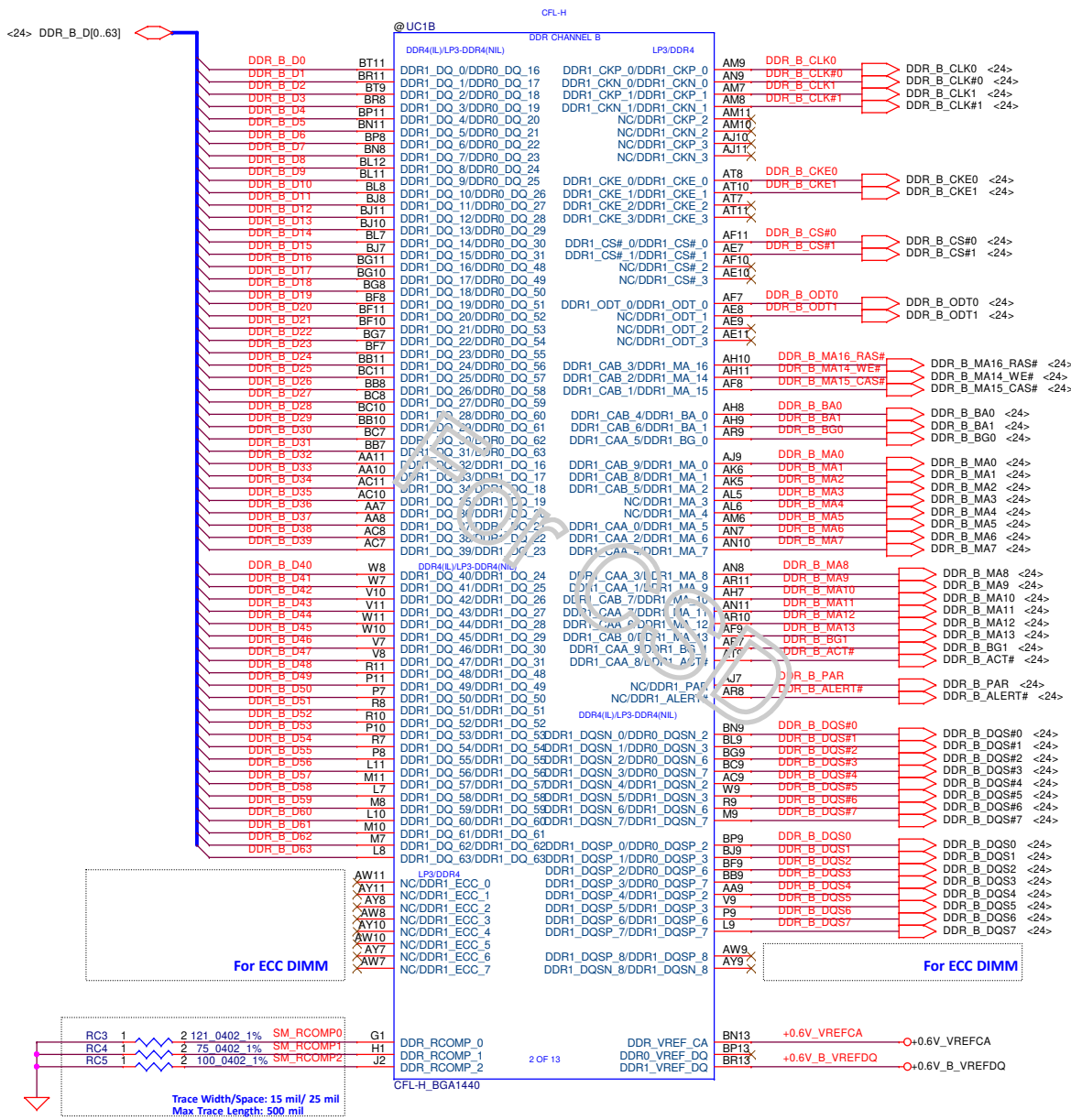
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										CFL-H(1/8)DDI/eDP	
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CHANNEL-B Interleaved Memory

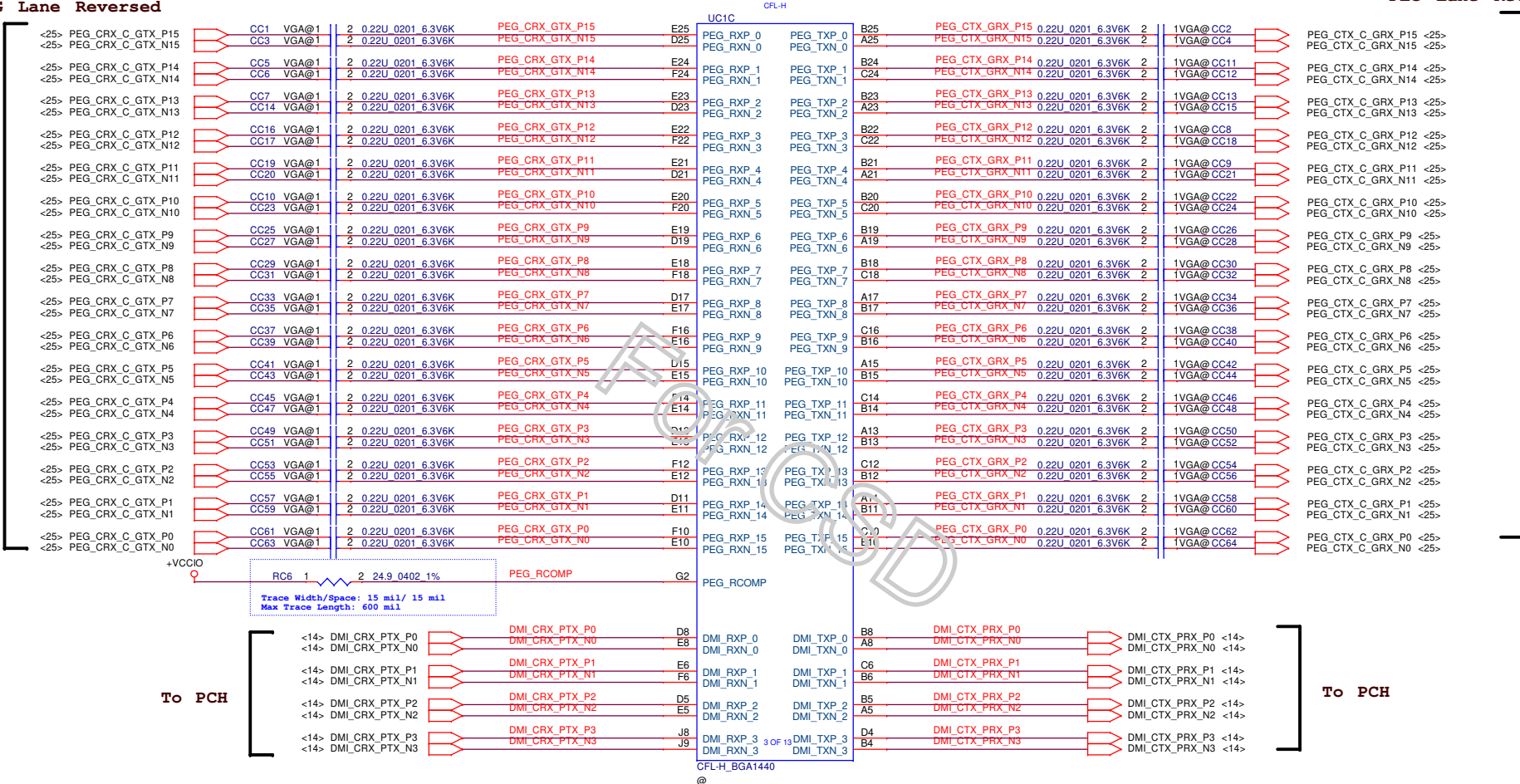


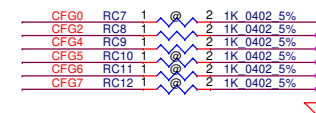
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PEG&DMI

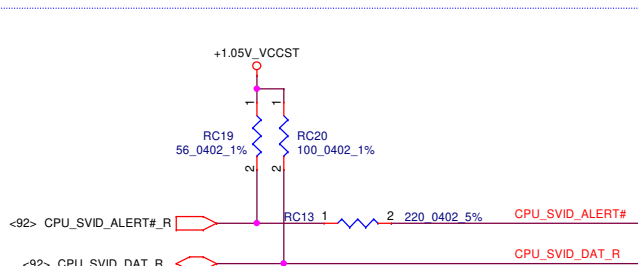
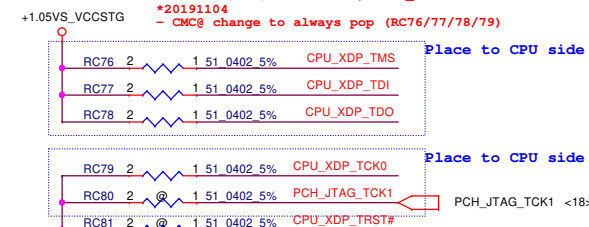
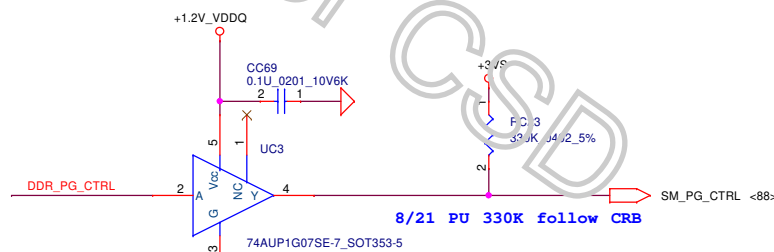
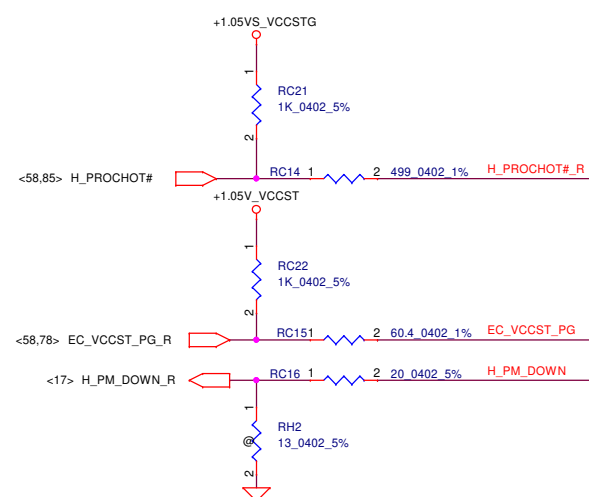
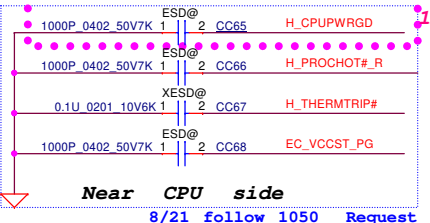
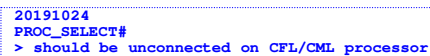
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



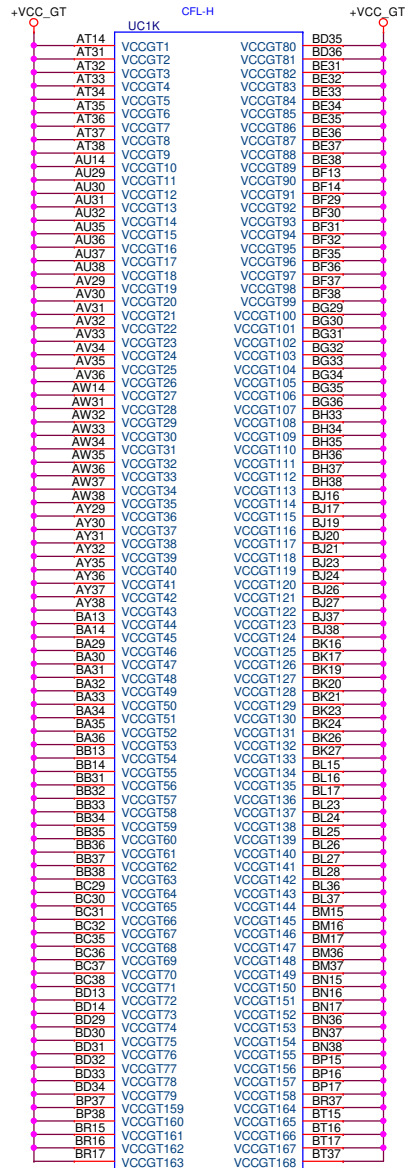


* CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation; 0 = Stall.
* CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation 0 = Lane numbers reversed.
* CFG[4]: eDP enable:
1 = Disabled. 0 = Enabled.
* CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
* CFG[7]: PEG Training:
1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.



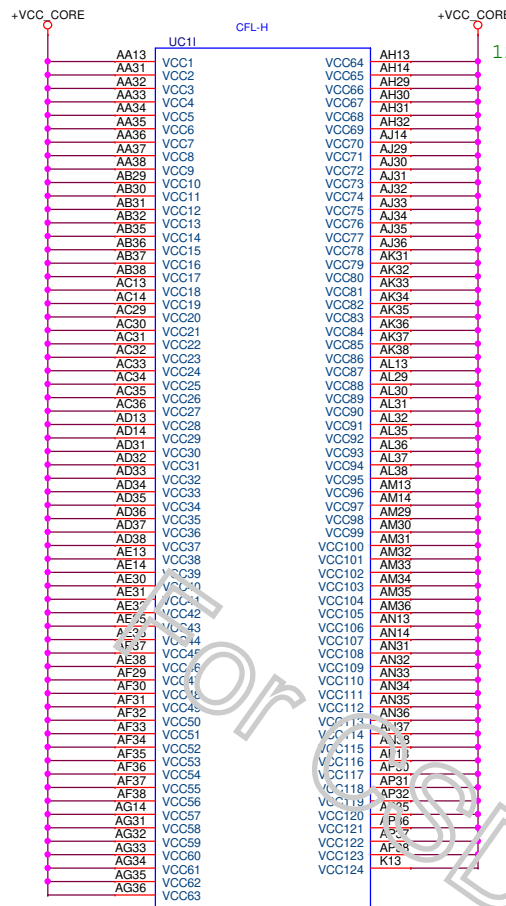
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GT
32000mA (Hexa Core GT2)



CFL-H_BGA1440
@

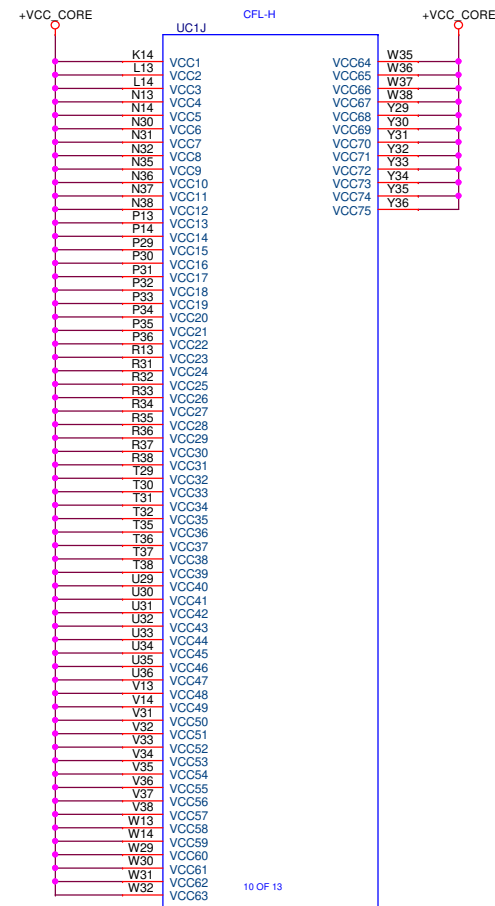
1. VccGT_Sense / VssGT_Sense Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



CFL-H_BGA1440
@

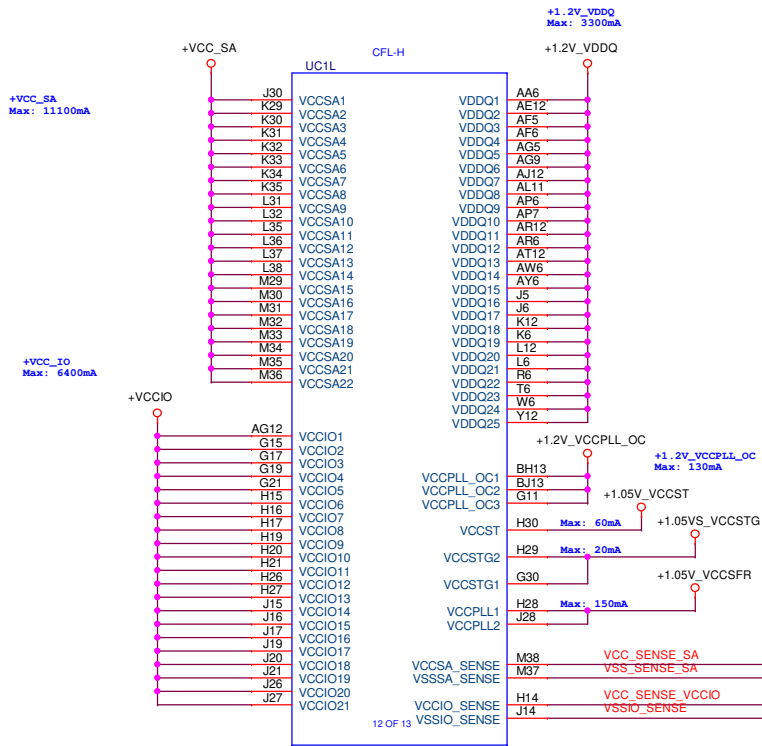
1. Vcc_SENSE / Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

128000mA (Hexa Core GT2)

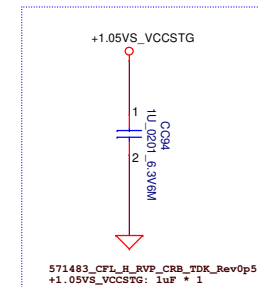
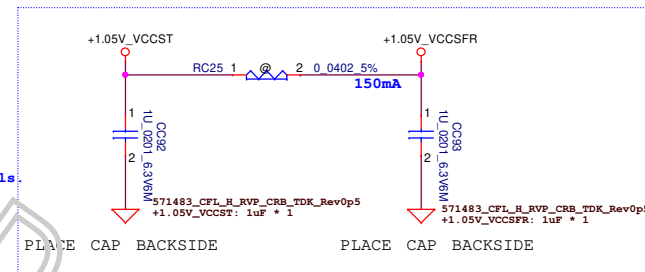
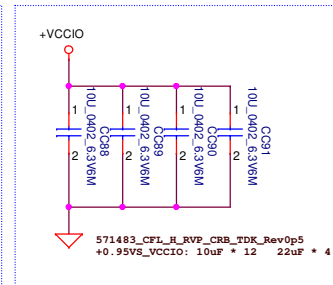
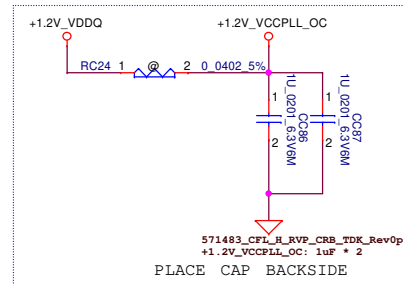
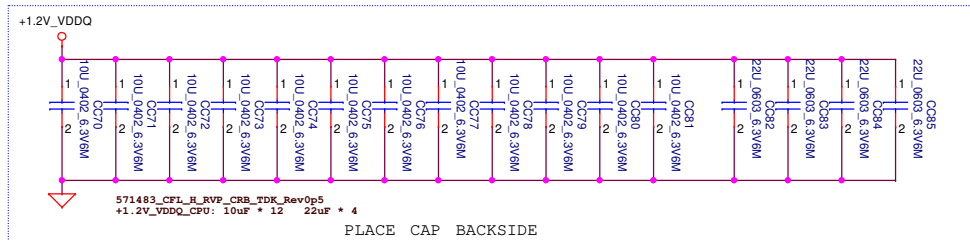


CFL-H_BGA1440
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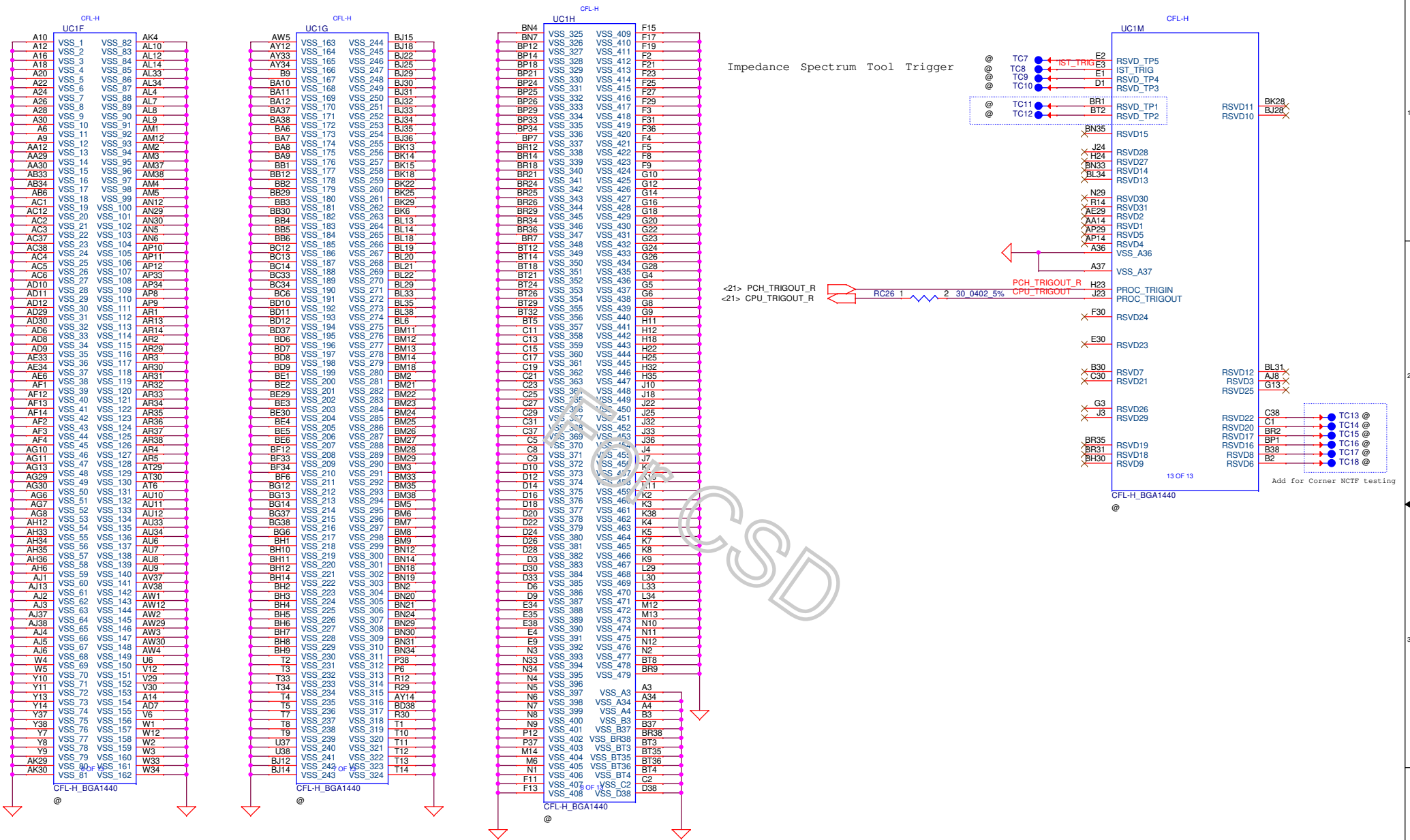
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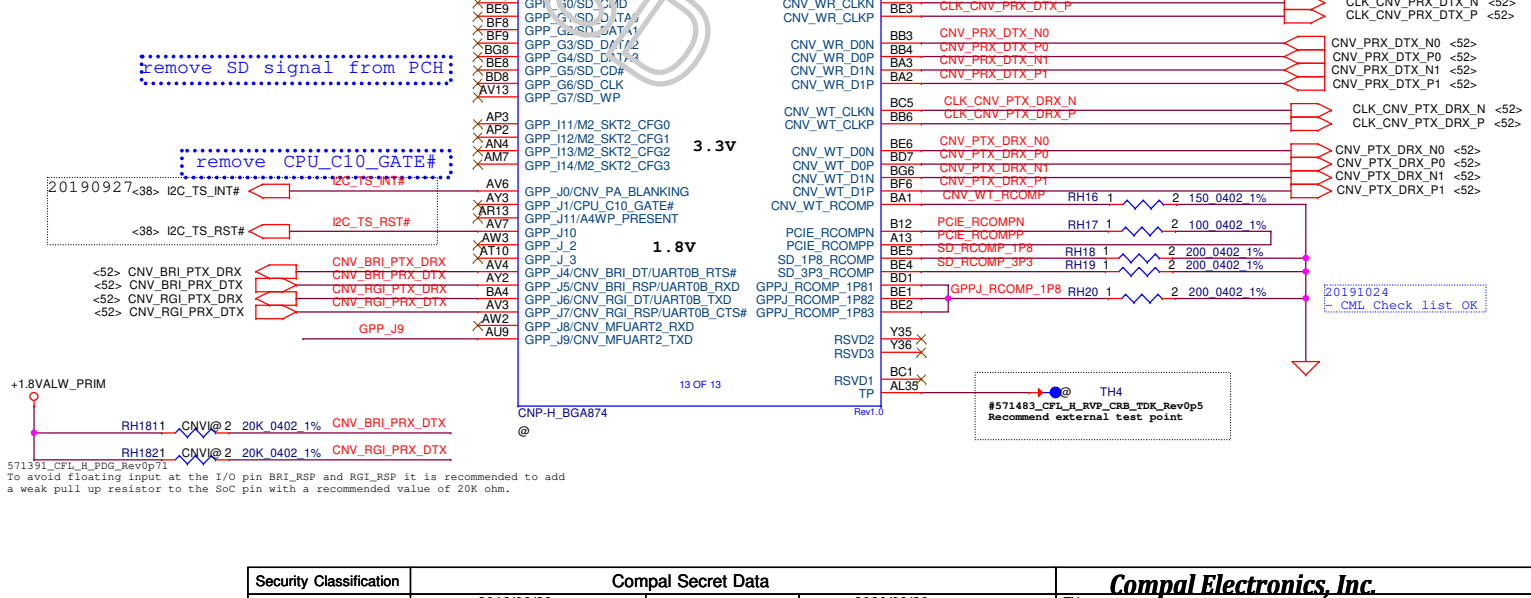
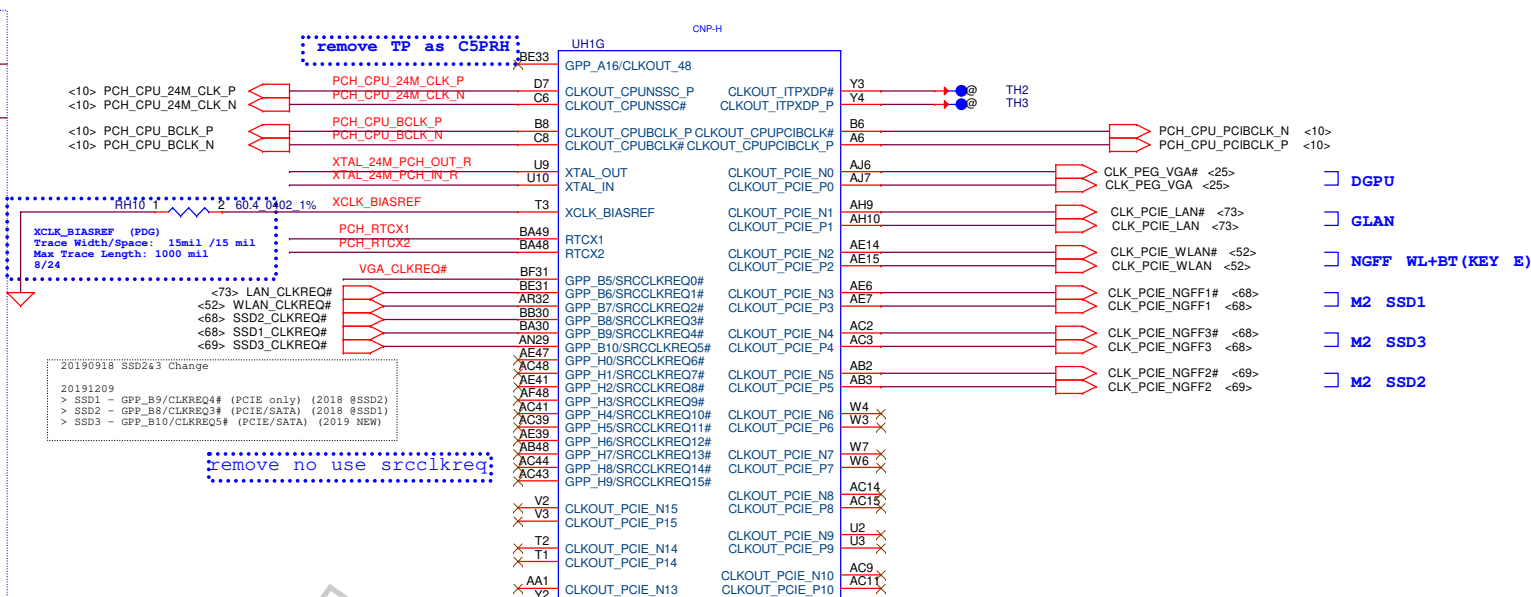
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



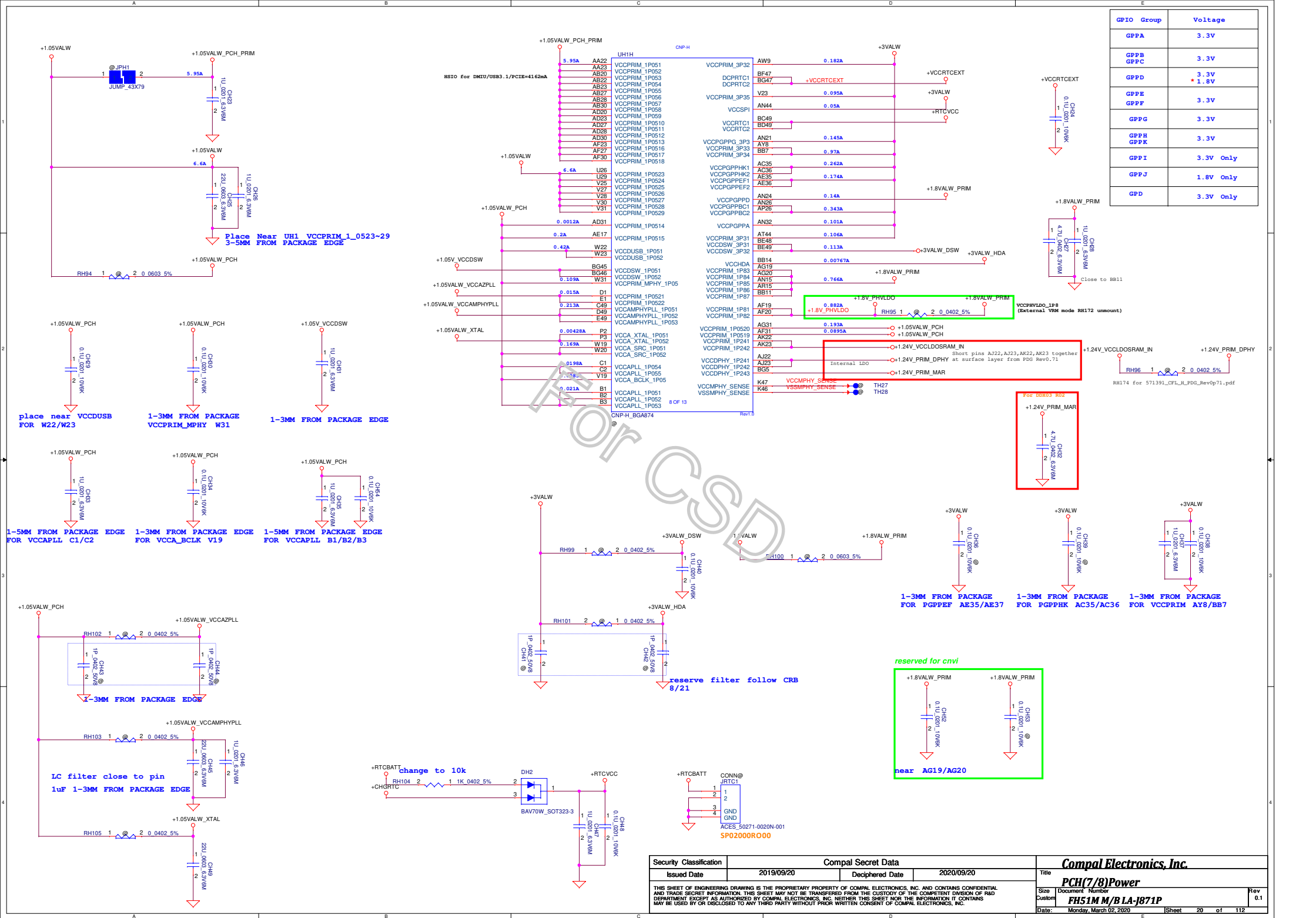
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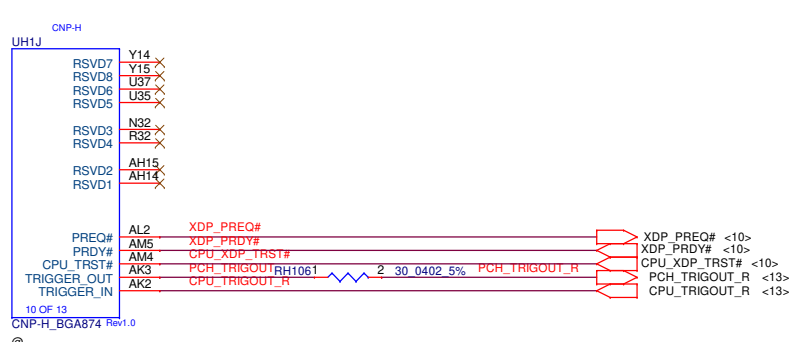
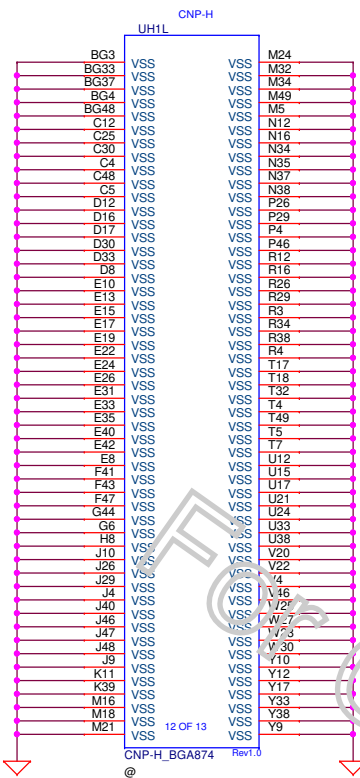
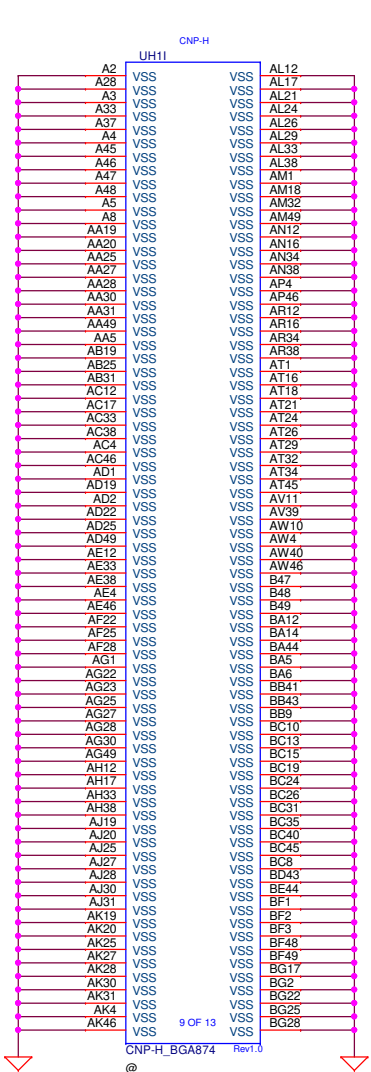


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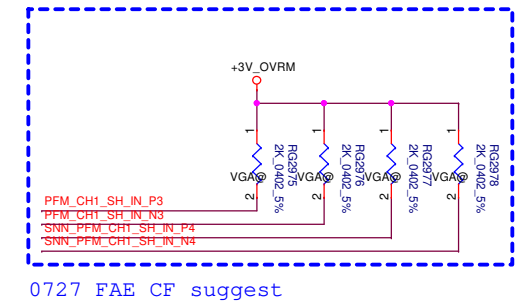
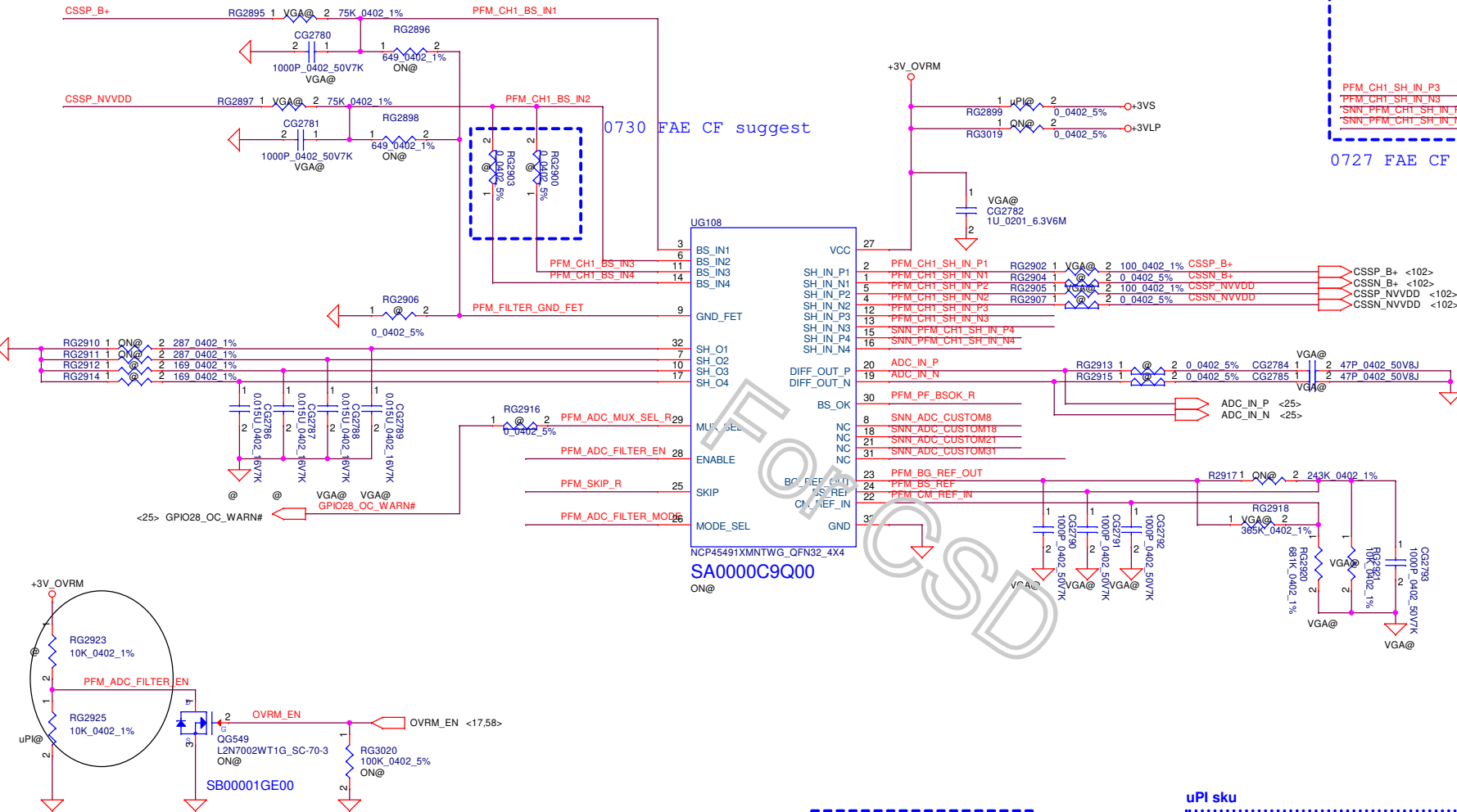


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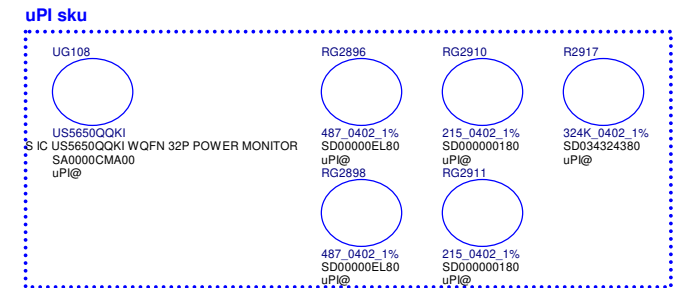
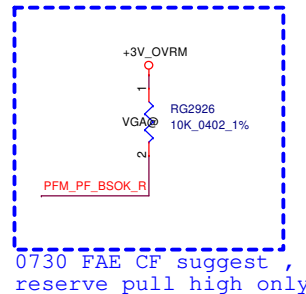
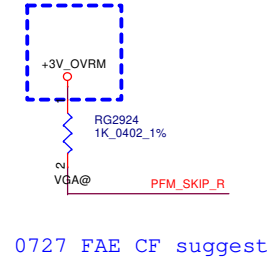
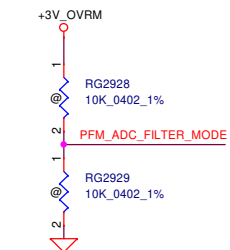




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ON semi : Add QG549 for S3/S4/S5
reduce power consumption when S3/S4/S5

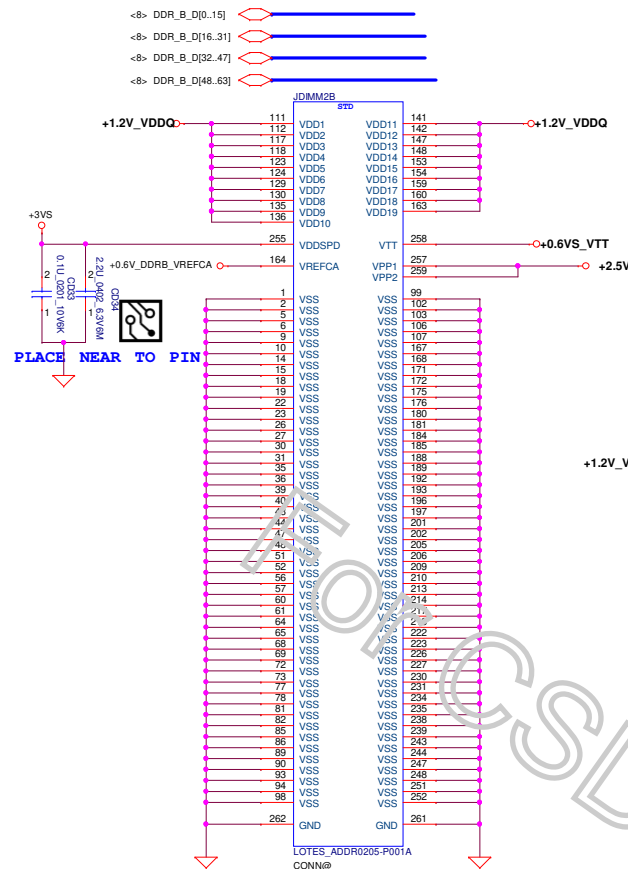


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> Non-ECC SO-DIMM

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> Non-ECC SO-DIMM



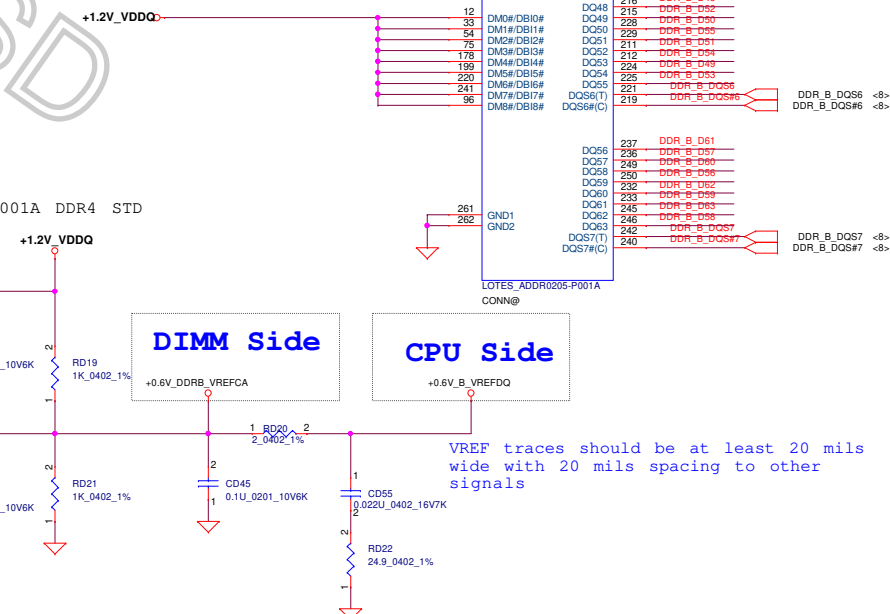
Two circuit diagrams illustrating the connection of a capacitor bank to a +1.2V_VDDQ supply.

Left Diagram (Parallel Connection): The capacitor bank is connected in parallel to the +1.2V_VDDQ supply. The capacitors are labeled as follows:

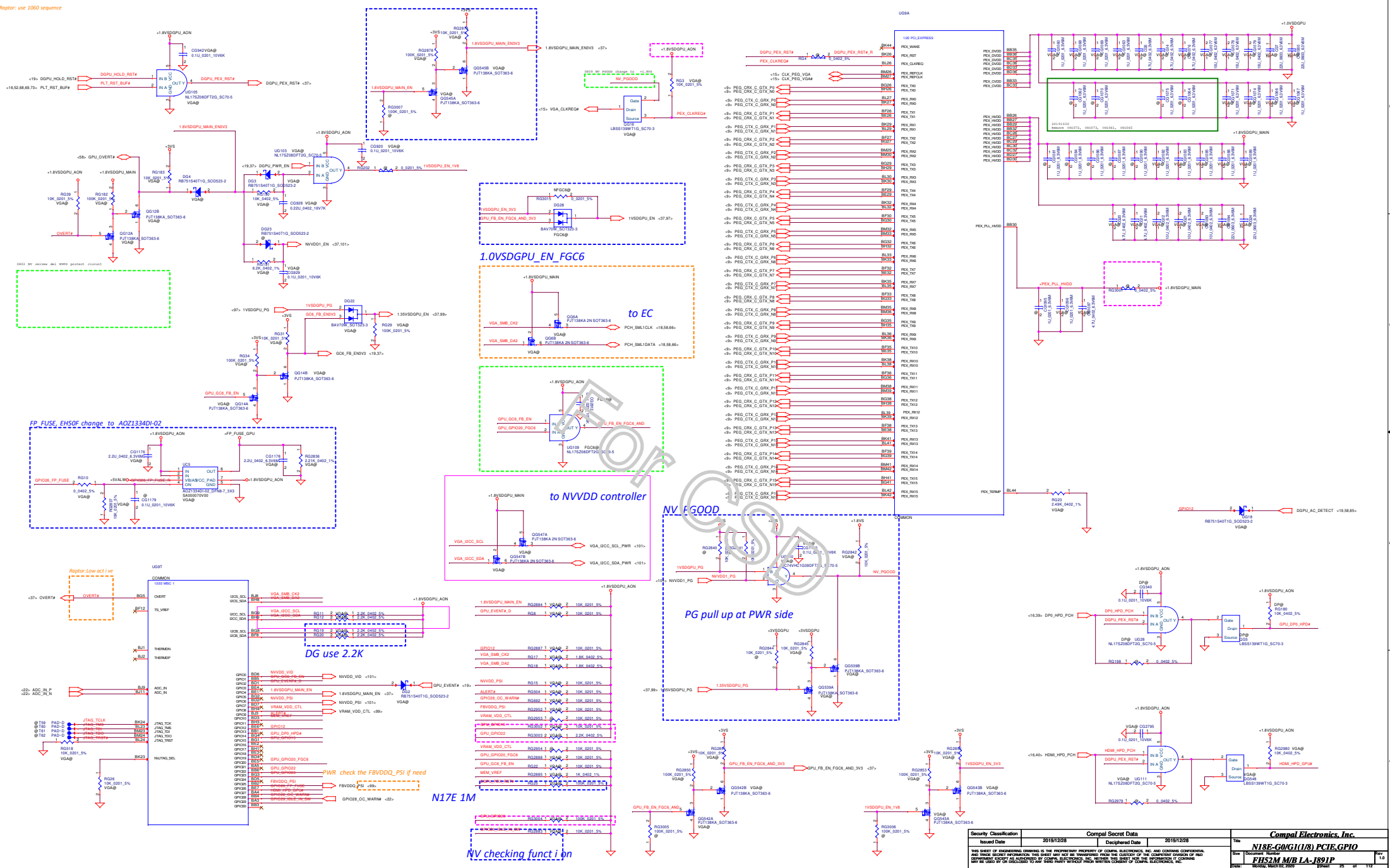
- 10uF*6 (CDS4, CDS5, CDS2, CDS3, CDS6, CDS7)
- 1uF*8 (CDS8, CDS9, CDS10, CDS11, CDS12, CDS13, CDS14, CDS15)
- 330uF*1 (CDS16)

Right Diagram (Series Connection): The capacitor bank is connected in series to the +1.2V_VDDQ supply. The capacitors are labeled as follows:

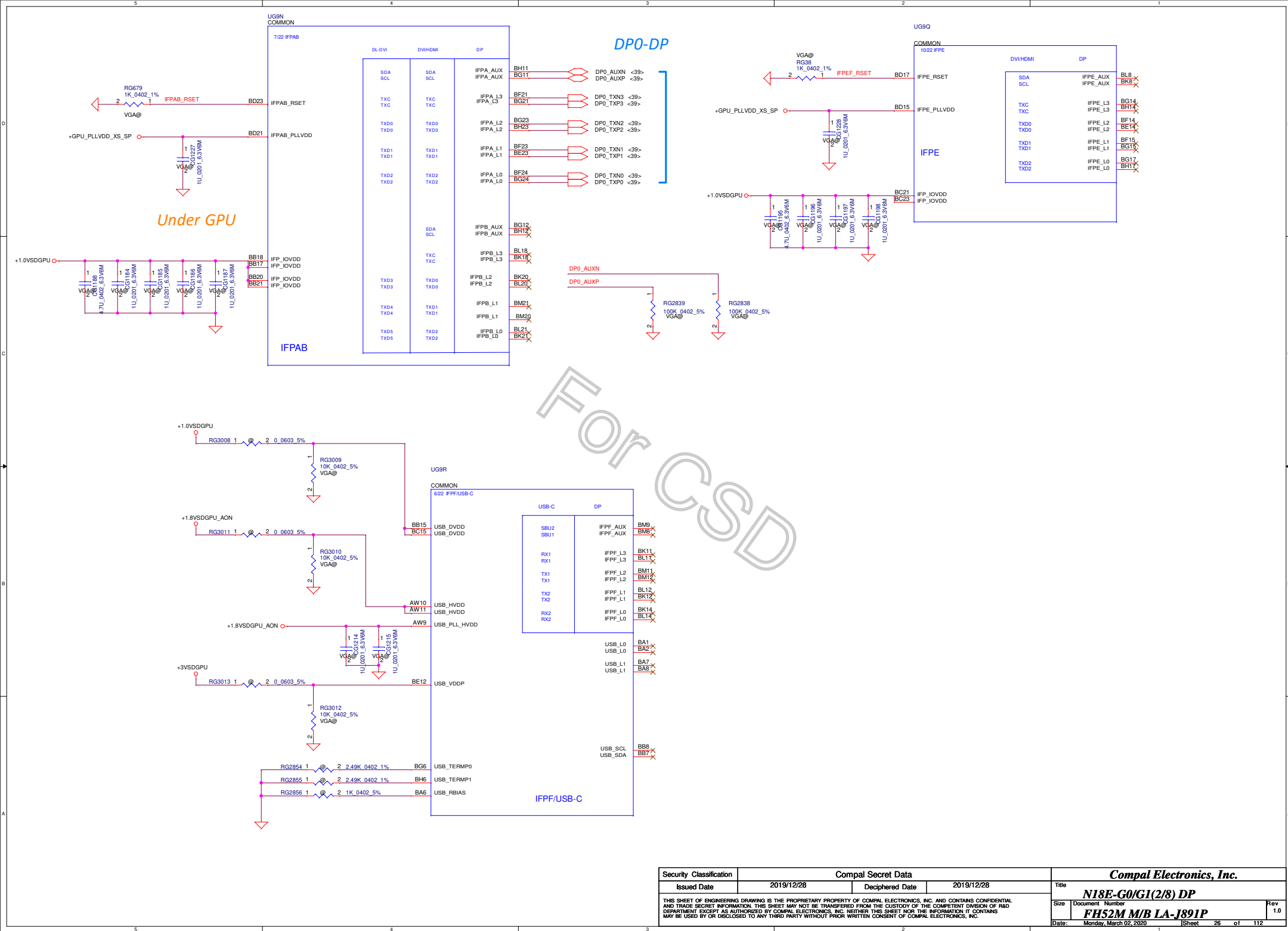
- 10uF*6 (CDS4, CDS5, CDS2, CDS3, CDS6, CDS7)
- 1uF*8 (CDS8, CDS9, CDS10, CDS11, CDS12, CDS13, CDS14, CDS15)
- 330uF*1 (CDS16)



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+FP_FUSE_GPU

+FP_FUSE_GPU

+1.8VSDGPU_AON

UG9F

UG9G

UG9H

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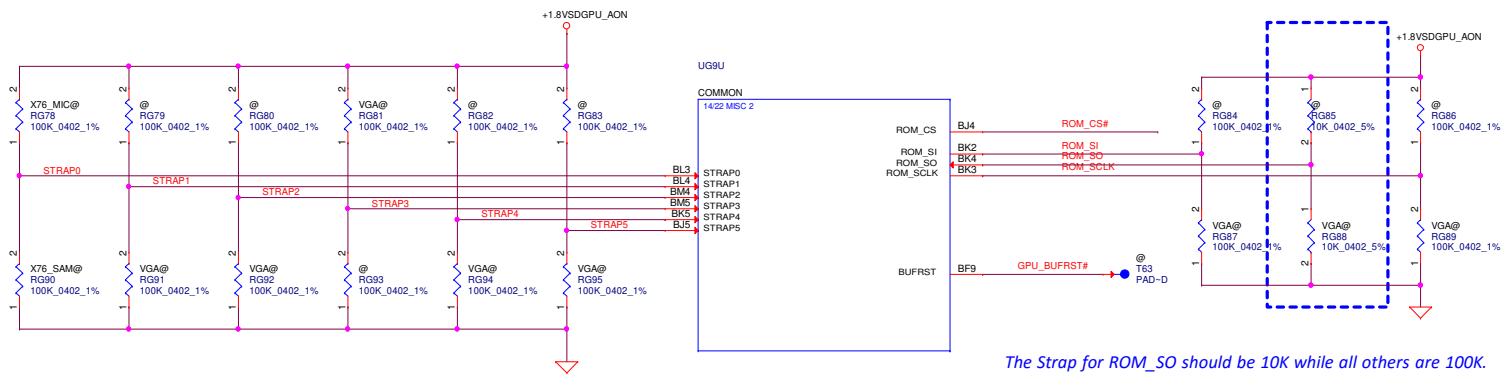
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Security Classification	Compal Secret Data			Title	
Issued Date	2019/12/28	Deciphered Date	2019/12/28	N18E-G0/G1(6/8) Power_GND	
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Date: Monday, March 02, 2020					Sheet 30 of 112

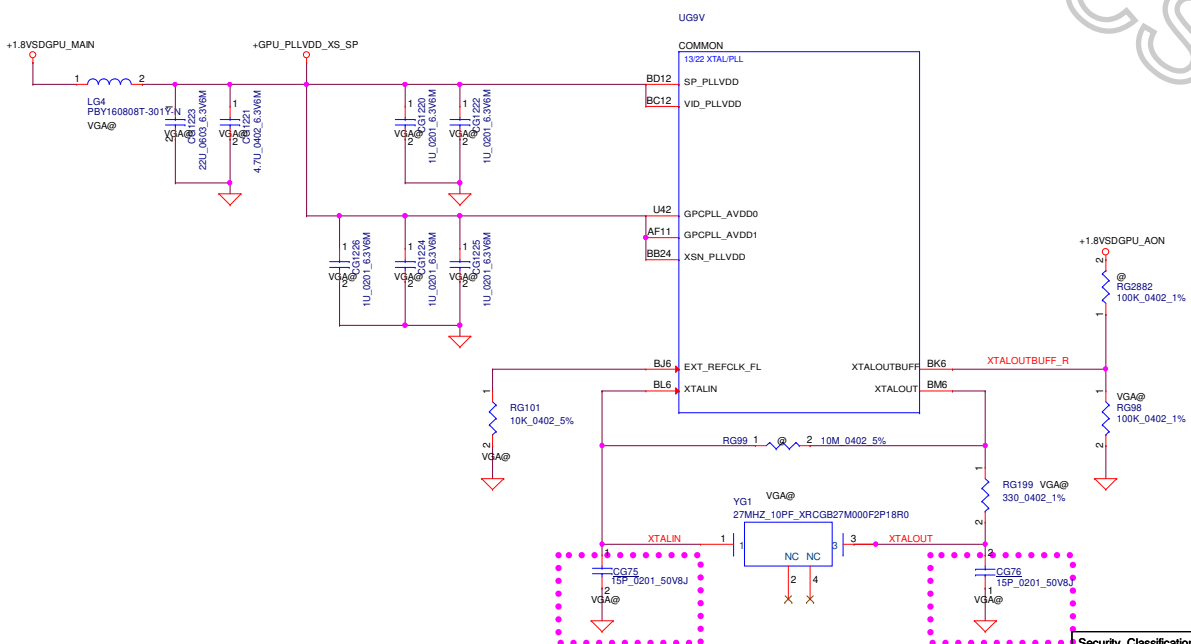
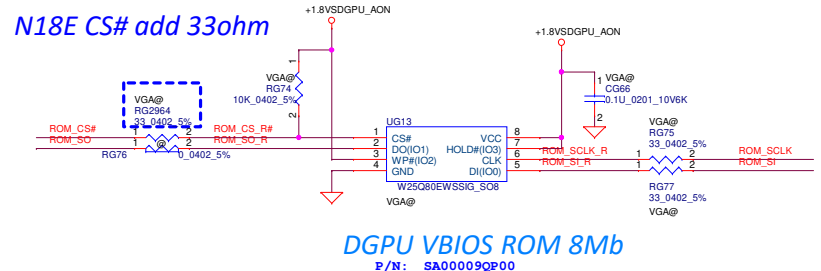


	(LSB)	(MSB)	(LSB)	(MSB)					
G-sync with VGA device	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	ROM_SO	ROM_SI	ROM_SCLK
Samsung K4Z80325BC-HC14	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PU 10kOhm	PD 100kOhm
MICRON MT61K256M32JE-14:A	PU 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PD 100kOhm	PD 10kOhm

Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density & GB	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Package	Memory Speed Grade	Date Code	Alert	RoHS Plan	Status
8 GB	2048/512x16	1.25V and 1.35V	Micro	M18E16D6M32JE-14:A	0x0	0x0	14 GDDR6	N/A	Full	Production	Production candidate

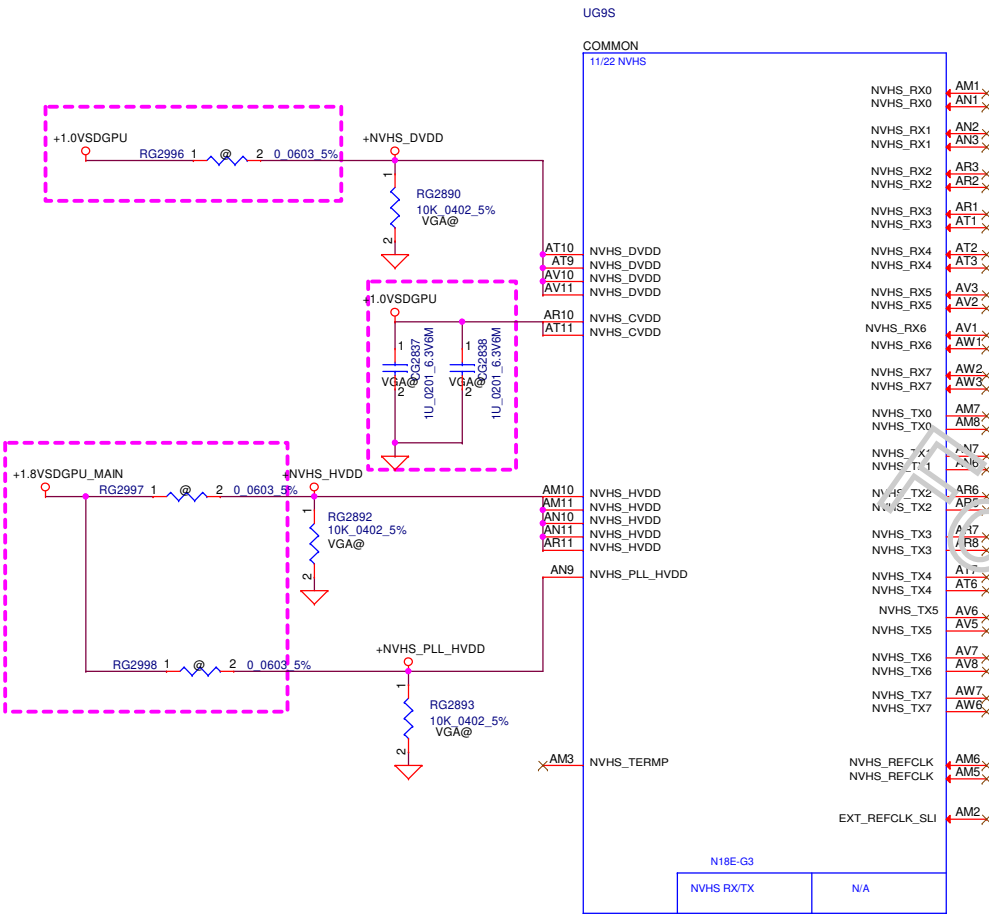
Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD



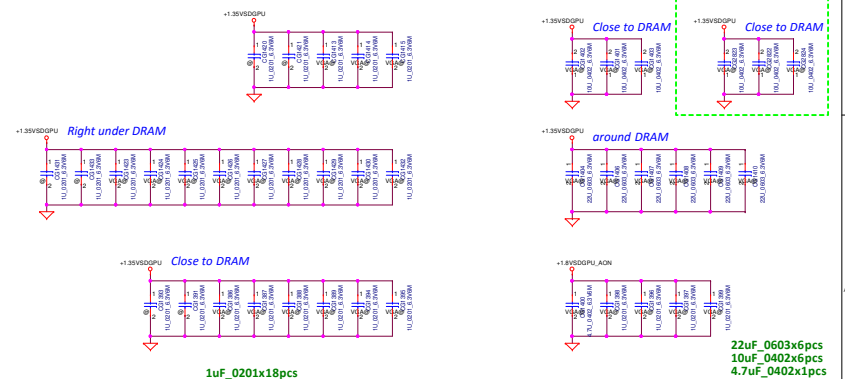
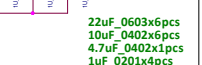
1A modify by ESD

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Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



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Size		Document Number			Rev
Date:		Monday, March 02, 2020			1.0
Sheet		32 of 112			

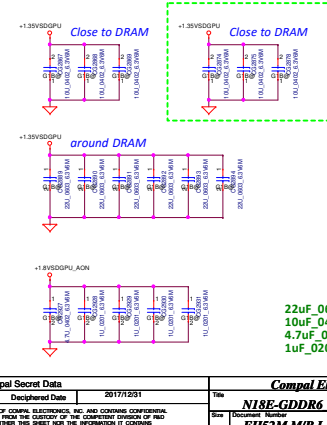
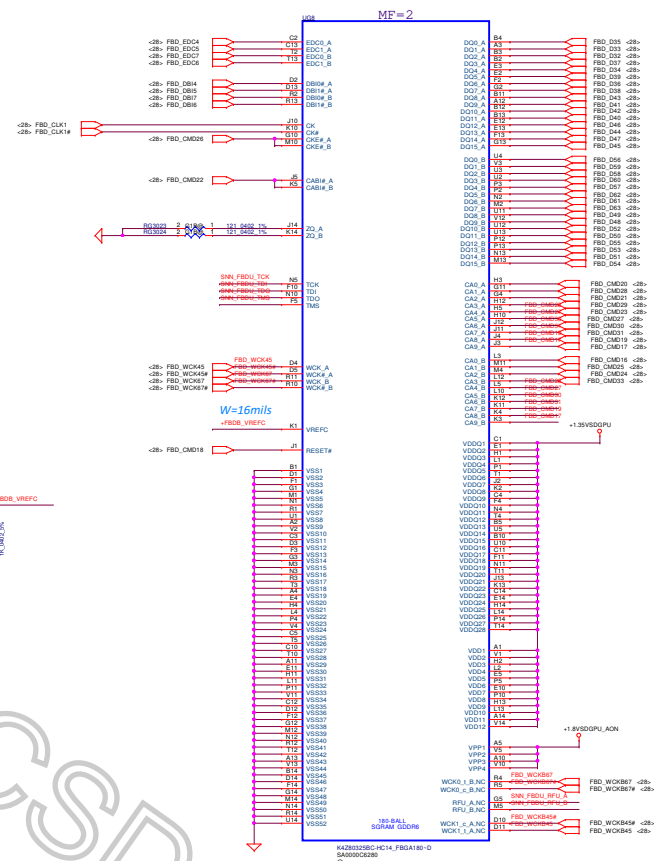


Note:

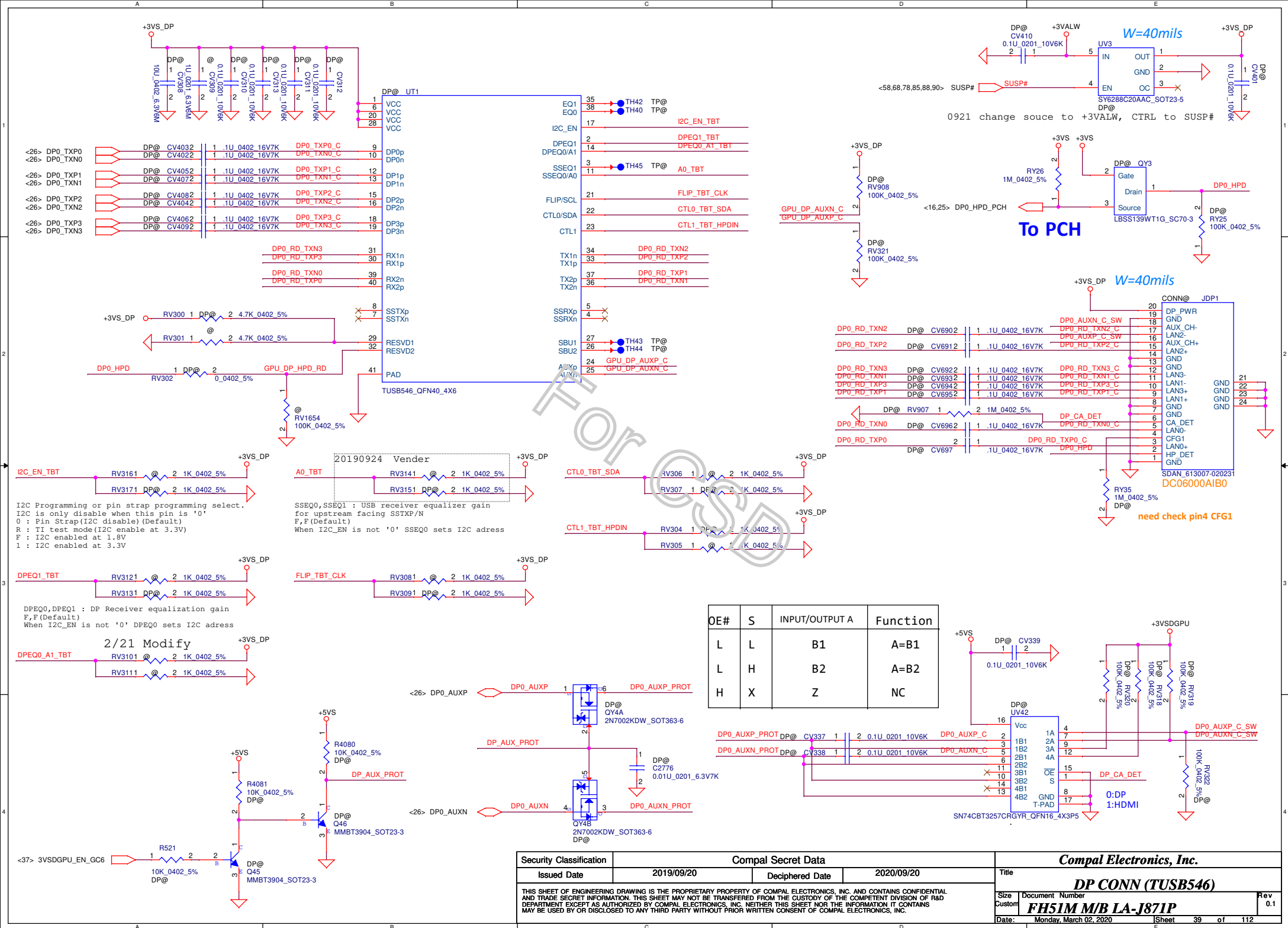
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

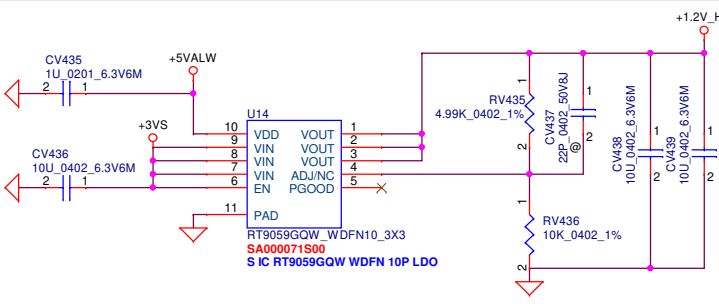
Note:

1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

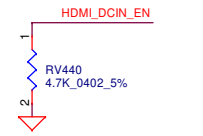


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Issued Date	2017/11/23	Deciphered Date	2017/12/31	Title N18E-GDDR6 D
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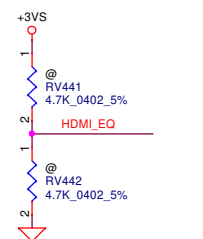




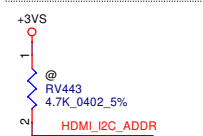
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default, AC coupling input



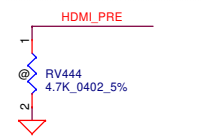
Receiver equalization setting (Internal 150K PD)
(*) L: programmable EQ for channel loss up to 5.3dB
() H: programmable EQ for channel loss up to 10dB
() M: programmable EQ for channel loss up to 14dB



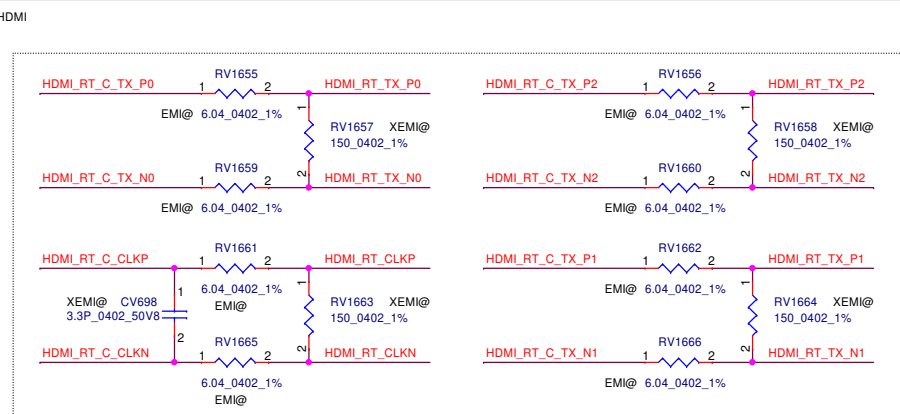
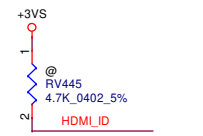
I2C Slave Address selection; Internal pull down; 3.3V I/O
L: Default, Slave address 0x10-0x2F
H: Alternative slave address 0x90-0x9F, 0xD0-0xDF.



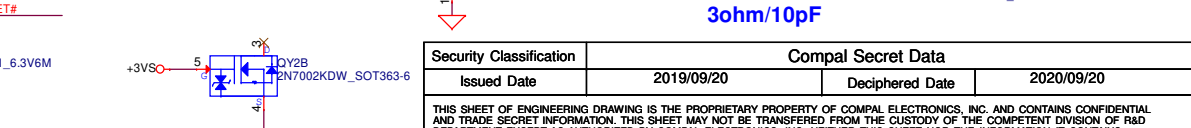
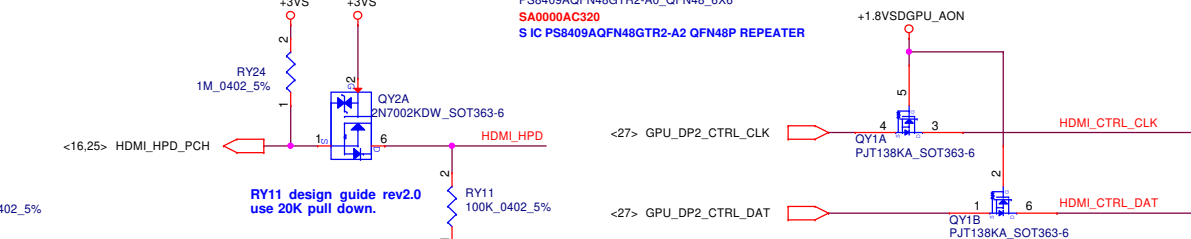
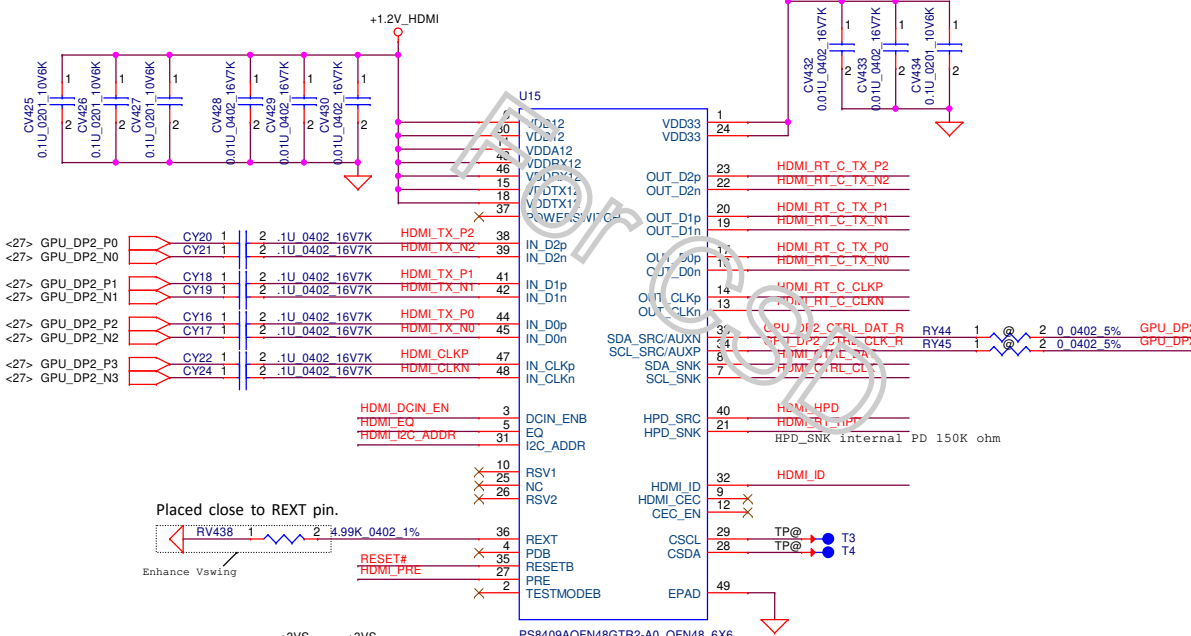
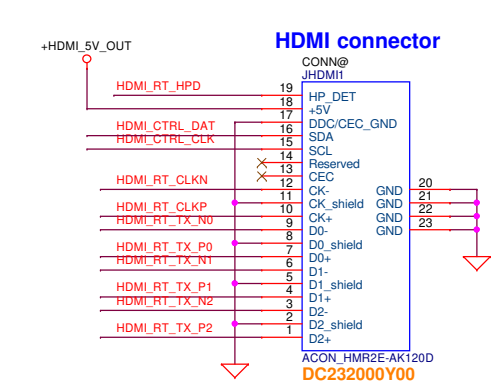
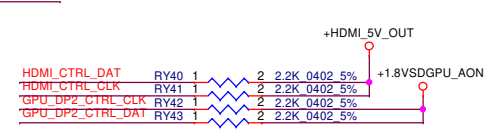
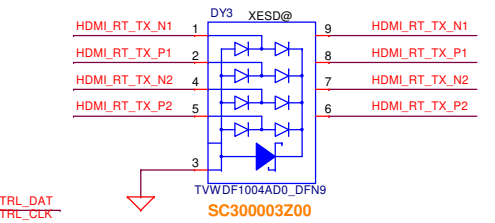
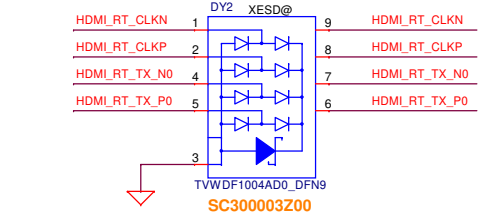
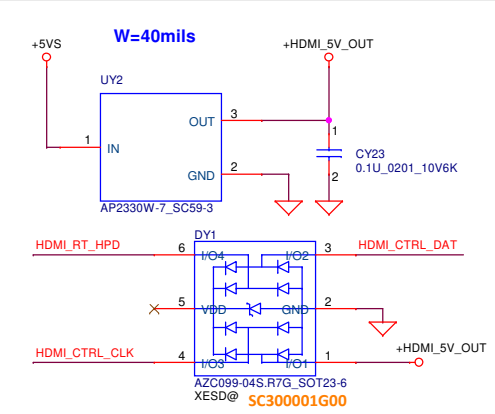
Output pre-emphasis setting; Internal pull-up 3.3V I/O
L: Pre-emphasis +2.5dB
H: Default, No Pre-emphasis



HDMI ID enable; Internal pull down; 3.3V I/O
L: Default, HDMI ID enable
H: HDMI ID disable



20191015, EMI



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Size	Document Number	Rev		FH52M M/B LA-J891P	
Custom		0.1			
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VRAM

N18E-G0

MICRON 1.35V

SAMSUNG 1.35V

GPU



N18EG0@
SA0000CK430
S IC D6 256M32 MT61K256M32JE-14-A ABO



N18EG1B@
SA0000DEX10
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



N18EG1R@
SA0000D4N40
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000BND10
S IC D6 256M32 MT61K256M32JE-14-A ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



SA0000C6210
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO

X76



X76L05@
ALT. GROUP PARTS MIC VRAM 6G FH51M
X76869BOL05



X76L06@
ALT. GROUP PARTS SAM VRAM 6G FH51M
X76869BOL06



X76L07@
ALT. GROUP PARTS MIC VRAM 8G FH51M
X76869BOL07



X76L08@
ALT. GROUP PARTS SAM VRAM 8G FH51M
X76869BOL08



X76L11@
ALT. GROUP PARTS MIC 1.35V VRAM 6G FH51M
X76869BOL11



X76L12@
ALT. GROUP PARTS SAM 1.35V VRAM 6G FH51M
X76869BOL12

OVRM



X76L09@
ALT. GROUP PARTS OVRM EG0G1G1R ON FH51M
X76869BOL09



X76L10@
ALT. GROUP PARTS OVRM EG0G1G1R UPI FH51M
X76869BOL10

N18E-G1B

MICRON 1.2V

SAMSUNG 1.2V



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO

N18E-G1R

MICRON 1.2V

SAMSUNG 1.2V



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



SA0000BND80
S IC D6 MT61K256M32JE-14-A 1.2V ABO



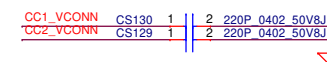
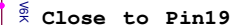
SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO



SA0000C6280
S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO

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				Date:	Monday, March 02, 2020
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				Rev	0.1

- Change to "with no Dual Role support"
- 5441E only uses the function of CC & Power SW



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

confirm realtek hand-shake

RTS441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

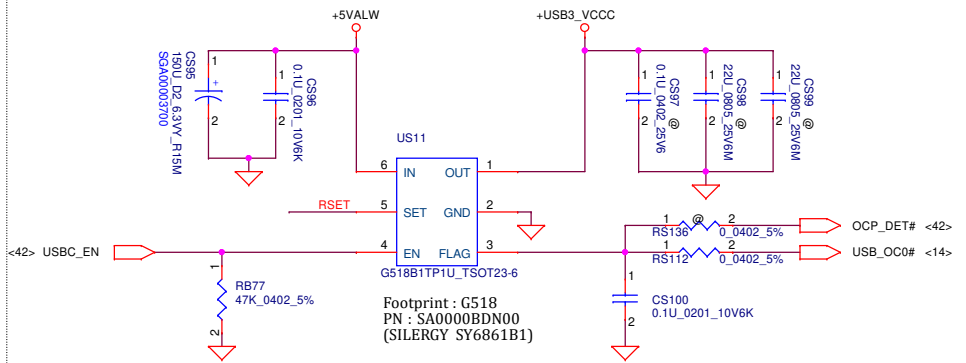
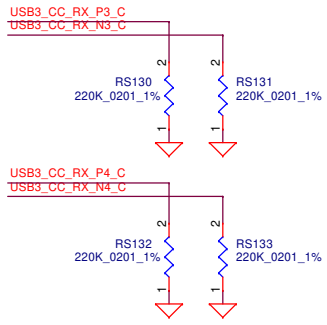
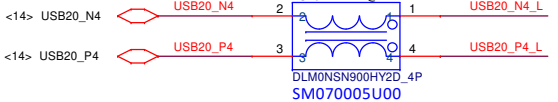
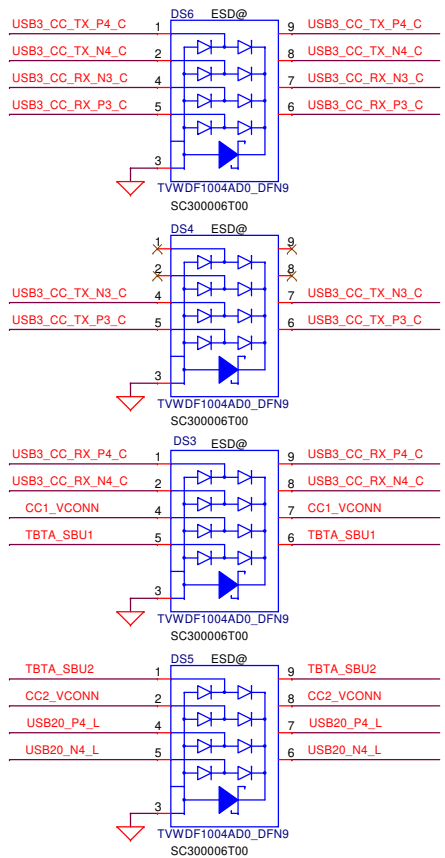


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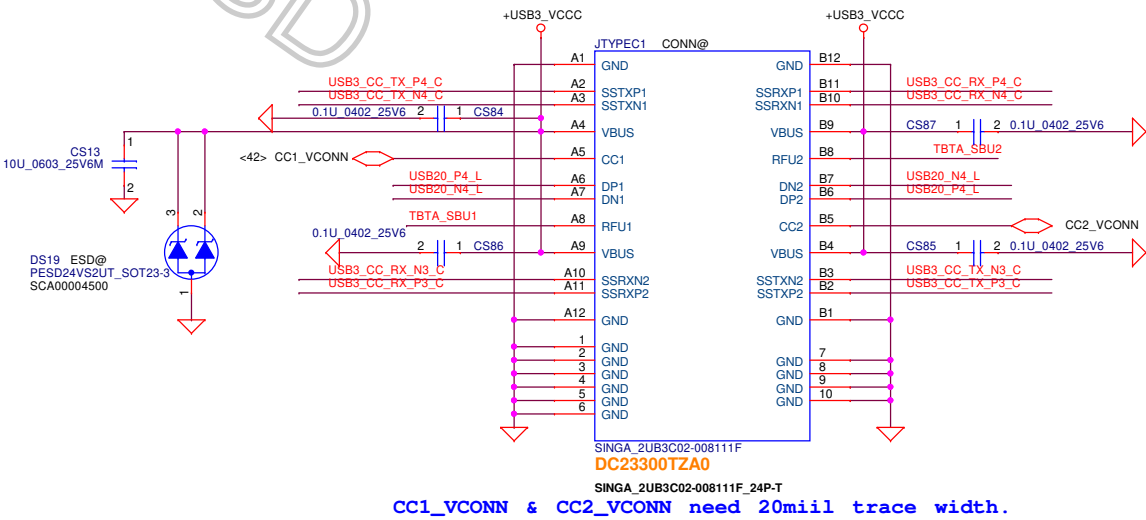
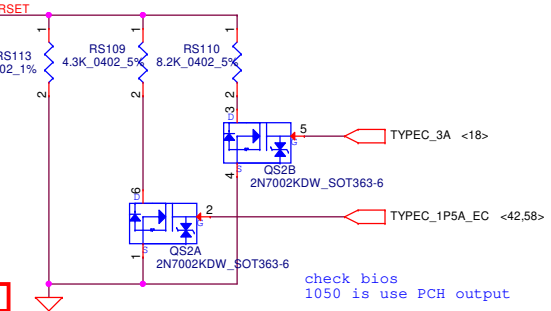
20191014
- Change to "with no Dual Role support"
- CS112/113/114/115 change to 0.33U

20191016
- USB3 Port5 change to Port3

20191015 - Pin SWAP for layout
20191016 For ESD request - Gen2 Solution SC300006T00



G518 MOS Current Limit					
GPP_B1 (TYPE_C_1P5A)	GPP_B4 (TYPE_C_3A)	RSET(kΩ)	MODE	limit point	
L	L	6.2	0.9A	1.09A	
L	H	3.53	1.5A	1.92A	
H	L	2.54	2A	2.67A	
*H	H	1.94	3A	3.5A	



CC1_VCONN & CC2_VCONN need 20mil trace width.

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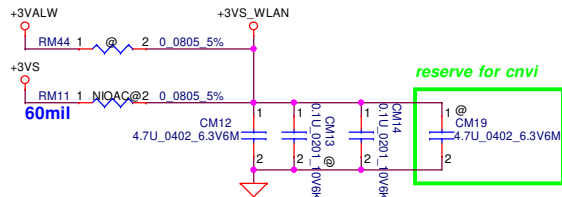
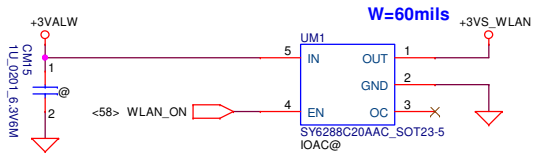
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20190918
LAN more to IO/B

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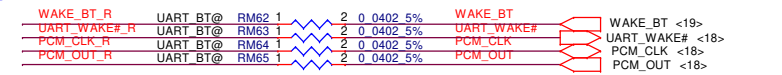
Wireless LAN



```
20191211 [FH51M CNVi review]
> RM69 change to 71.5k & CNVi@
> RM70 set CNVi@
> RH22 change to 20K
> RM36/RM37/RM67/RM68 change to 22 ohm
> RM16 recommend to 4.7k (no action)
> RH199 recommend to pop (no action)
> RM45 recommend to 10K (no action)
> WL_OF# recommend to PU 10K (no action)
```

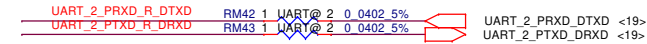
```
20191209 [FH5VF CNVi review]
Pin10 - RM41 Close to PCH
Pin14 - CLKREQ_CNV# PD RM69
Pin20 - UART_WAKE PU RM70(4)
Pin22 - RM36@M.2 / RH181@PCH
Pin32 - RM37@PCH / RH22@M.2
Pin34 - RM67@M.2 / RH182@PCH
Pin36 - RM68@PCH / RH15@M.2
```

UART BT

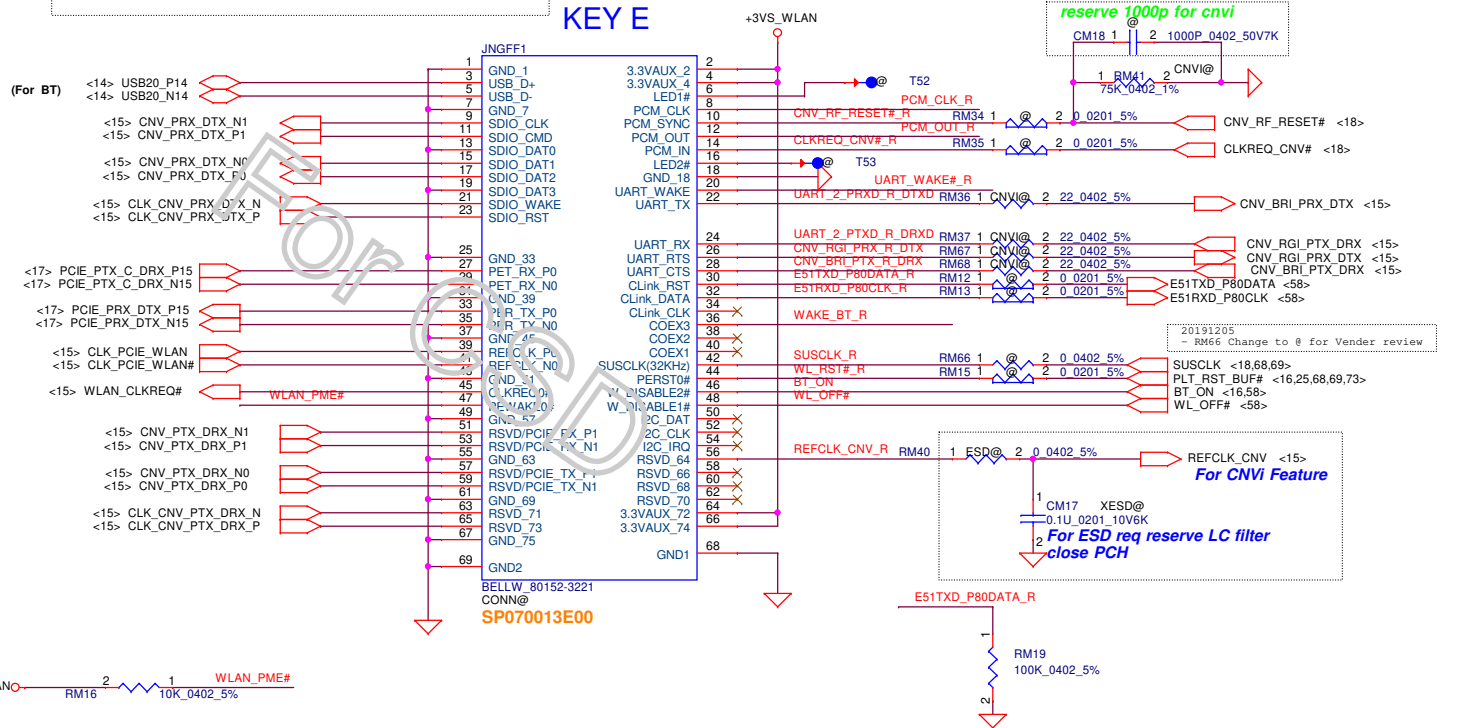


20191007
- Add RM62/63/64/65

Co-layout with CNVi for SW debug



KEY E



NGFF WL+BT (KEY E)

74	1.BV	GND	75
70	1.BV	RESERVED/REFCLKIN1	78
72	1.BV	RESERVED/REFCLKUP1	71
68	UM_Power_SBC/GPIO/PENALIN#	GND	69
66	UM_Power_SBC/CLKREQ1#	Reserved/PERn1	67
64	UM_SWP/PERST1#	Reserved/PERP1	65
62	RESERVED	GND	63
60	ALERT# (IO(0.3.BV)	Reserved/PETr1	61
58	QCC CLK (IO(0.3.BV)	Reserved/PETP1	59
56	QCC DATA (IO(0.3.BV)	GND	57
54	WL_DISABLE1 (IO(0.3.BV)	PENALIN# (IO(0.3.BV)	55
52	Reserved/W_DISABLE1 (IO(0.3.BV)	CLKREQ0 (IO(0.3.BV)	53
50	PERST0# (IO(0.3.BV)	GND	51
48	SUSCLK32MHz (IO(0.3.BV)	REFCLKIN0	49
46	CODEX1 (IO(0.1.BV)	REFCLKUP0	47
44	CODEX2 (IO(0.1.BV)	GND	45
42	CODEX3 (IO(0.1.BV)	PETr0	43
40	VENDOR DEFINED	PERP0	41
38	VENDOR DEFINED	GND	39
36	VENDOR DEFINED	PETr0	37
34	UART1 RTS (IO(0.1.BV)	PETP0	35
32	UART1 CTS (IO(0.1.BV)	GND	33
30	UART1 Tx (IO(0.1.BV)	UART1 Rx (IO(0.1.BV)	31
28	UART1 Rx (IO(0.1.BV)	UART1 Tx (IO(0.1.BV)	29
26	UART Wakeup (IO(0.3.BV)	SIO2 Wakeup# (IO(0.1.BV)	23
20	GND	SIO2 Wakeup (IO(0.1.BV)	21
18	GND	SIO2 DATIN0 (IO(0.1.BV)	17
16	LED#1 (I/O0)	SIO2 DATIN1 (IO(0.1.BV)	15
14	PC0M_OUT/IS25_OUT (IO(0.1.BV)	SIO2 DATI0 (IO(0.1.BV)	13
12	PCM_IN/IS25_S0_IN (IO(0.1.BV)	SIO2 CMV0 (IO(0.1.BV)	11
10	PCM_SYNC/IS25_WS (IO(0.1.BV)	SIO2 CMV1 (IO(0.1.BV)	9
8	PC0M_CLK/IS25_SCK (IO(0.1.BV)	SIO2 CLK0 (IO(0.1.BV)	7
6	LED#1 (I/O0)	GND	6
4	1.BV	USB_D-	5
2	1.BV	USB_D+	3
		GND	1

(link to PICE Port 3)
PCIE X1

(From PCH CLKOUT2)
PCIE CLK

reserve for BT_ON OD pull high (1.0)



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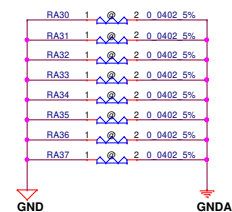
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DMIC_DATA 2 1 R41 0.0402_5% DMIC_DATA_R 1 DMIC_DATA_R <38>

<18> PCH_DMIC_DATA0 PCH_DMIC_DATA0 R43 1 33.0402_5%

<18> PCH_DMIC_CLK0 PCH_DMIC_CLK0 R44 1 33.0402_5%

DMIC_CLK 2 1 R45 100k_0402_5% DMIC_CLK_R 1 DMIC_CLK_R <38>

TO eDP cable

Change PN to SM01000Q500

20191008
- change to unpop

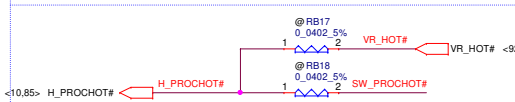
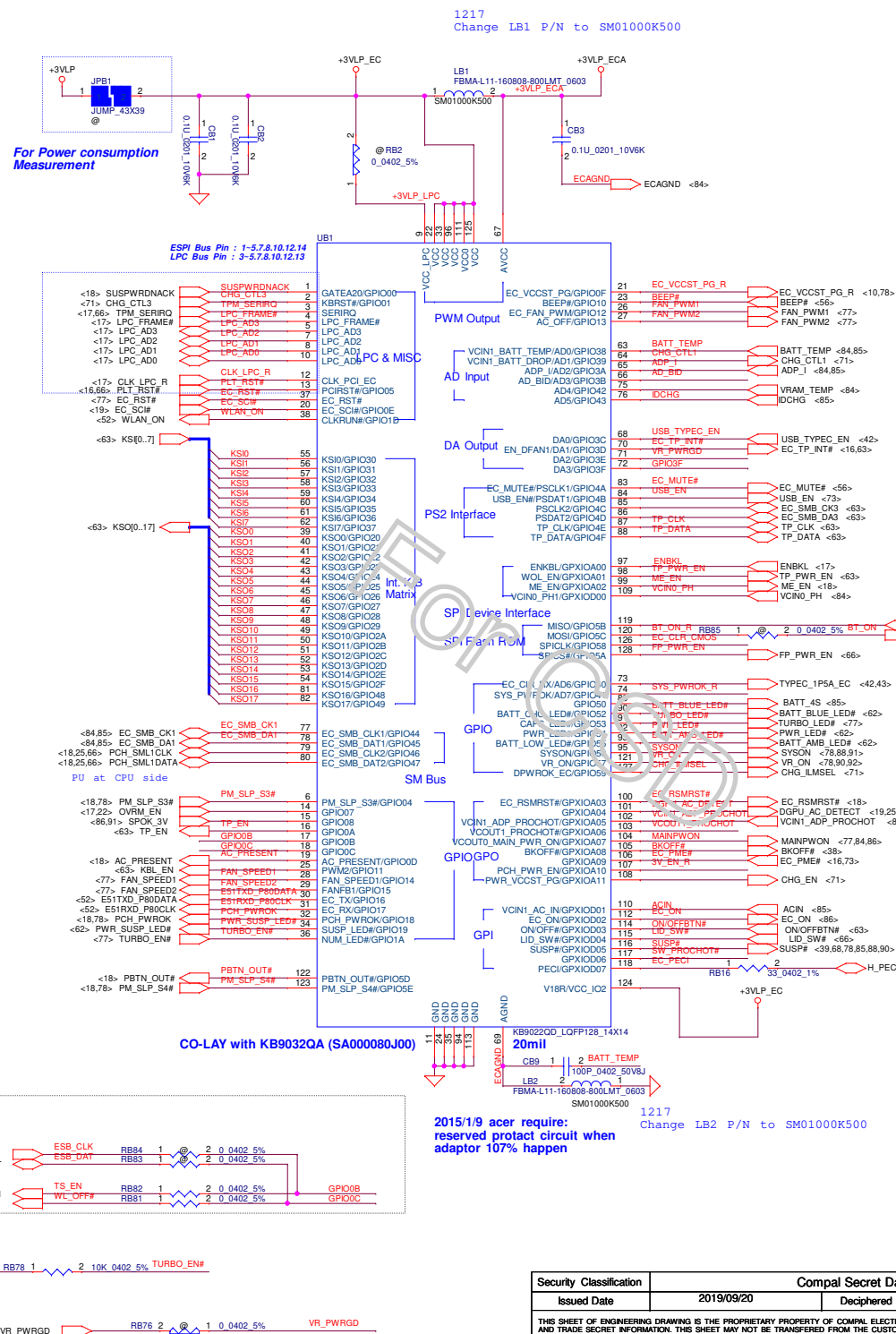
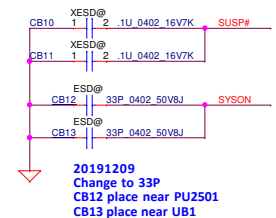
Fallow Raptor

<58> BEEP# RA3# 2 22k 0402 5% BEEP# R CA3# 1 2 0.1u 0201 10V6K
 <18,19> PCH_SPKR RA3# 2 22k 0402 5%
 @ CA37 1 RA40
 100P_0402_50VB7 2 5.1K_0402_1%
 1008
 39/RA38 change to 22k
 40 change to 5.1k

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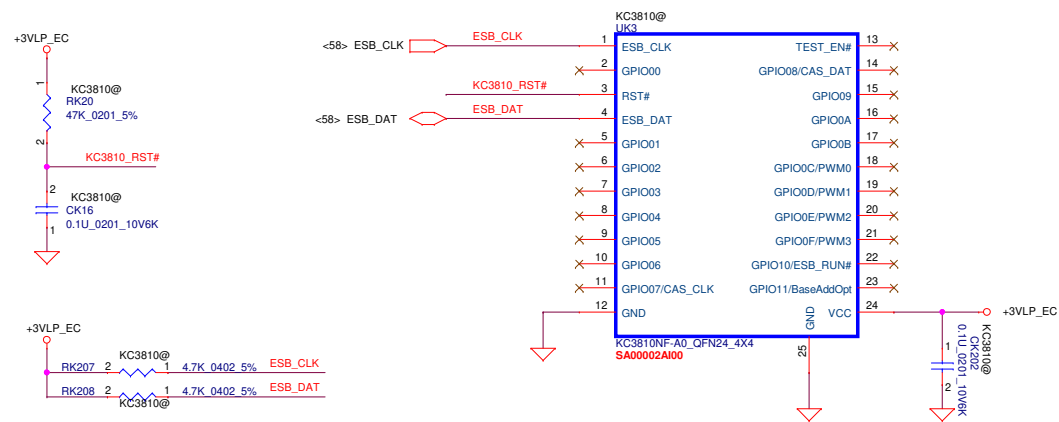
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*NMI_DBG#; is a debug pin for EC to
infrom BIOS after press hot key.
OMEN New ESB CLK&DAT for Extend I/O



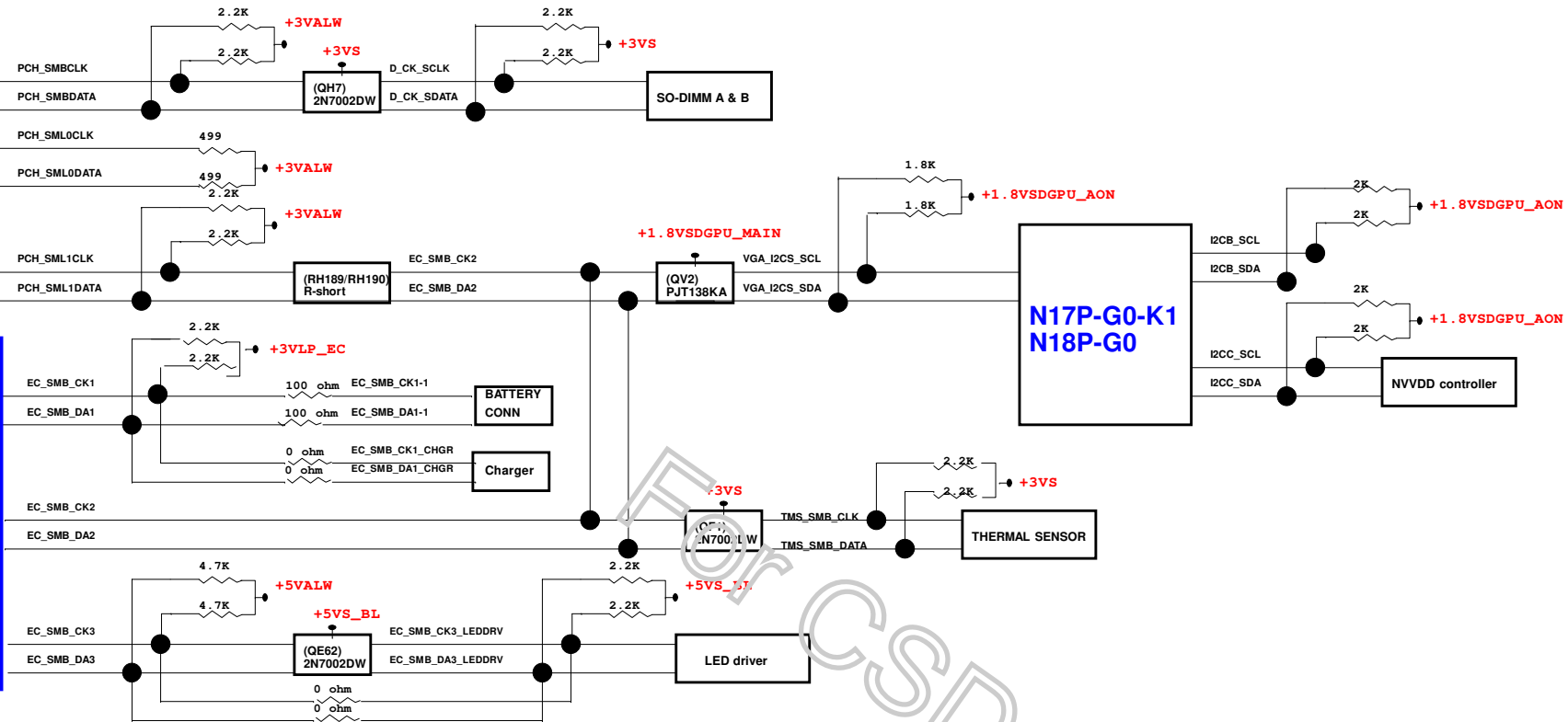
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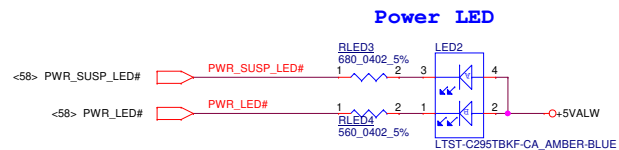
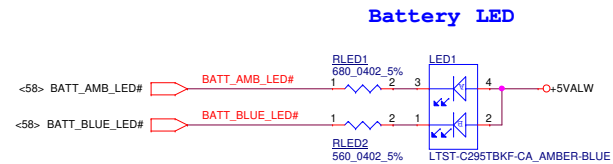
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Cannonlake
PCH - H

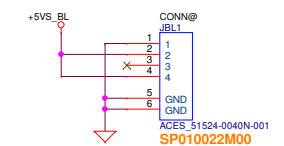
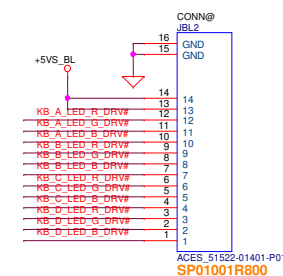
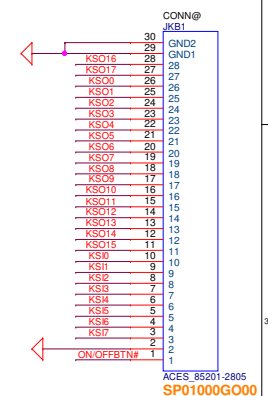
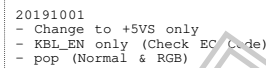
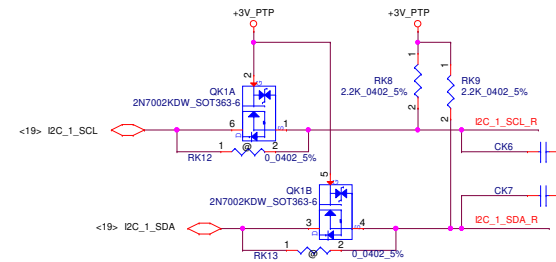
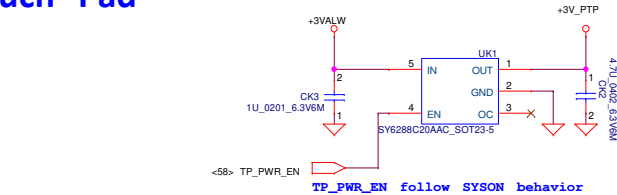
KB9022





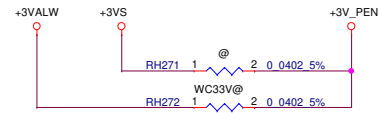
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	LED
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				Date:	Monday, March 02, 2020
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Touch Pad

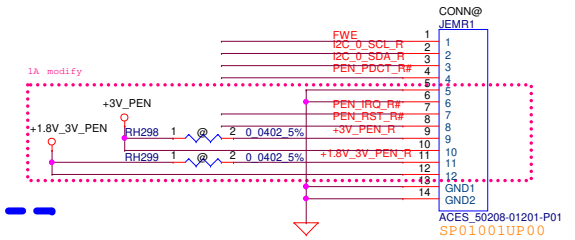


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	
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				Document Number	0.1
				FH51M MB LA-J871P Date: Monday, March 02, 2020 Sheet 63 of 112	

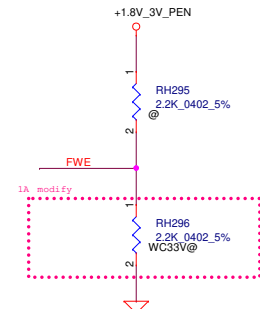
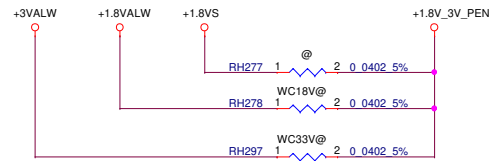
3V_PEN



EMR

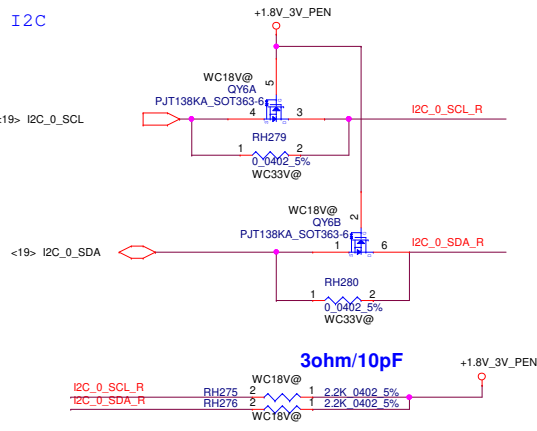


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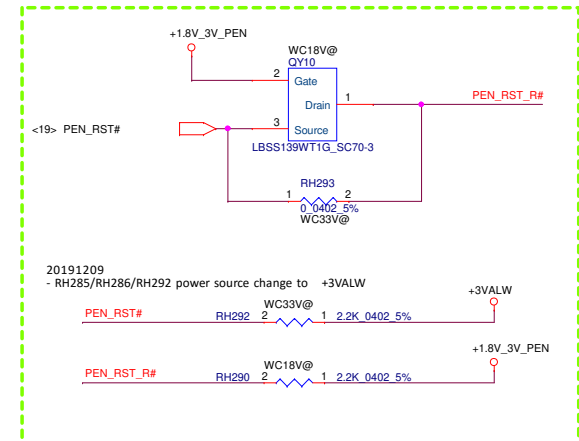
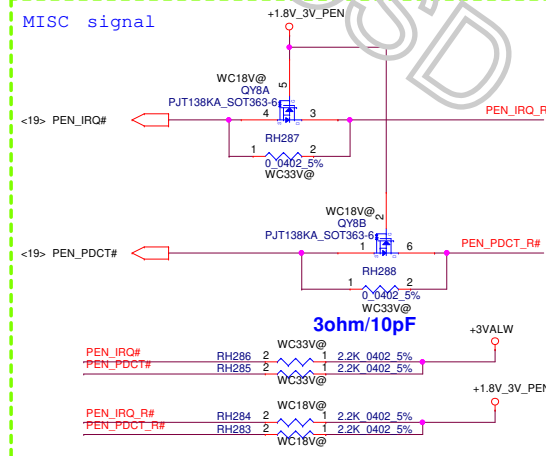


20191008
- QY6/QY8 change to SB000016K00
Default use 0ohm(WC33V@)

I2C



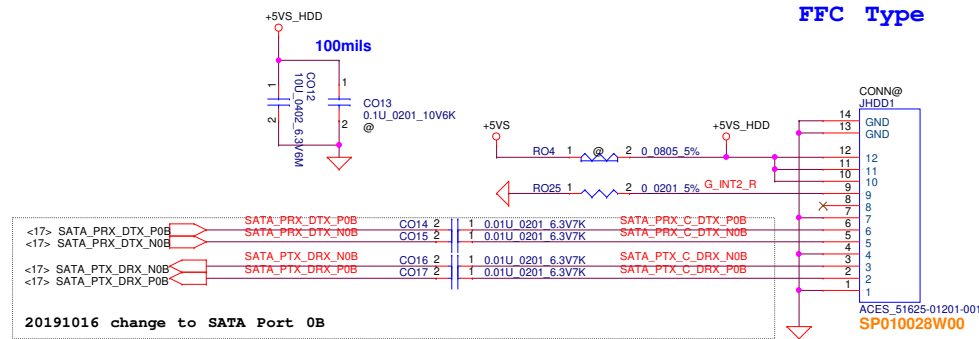
MISC signal



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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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				Date: Monday, March 02, 2020	Sheet 65 of 112

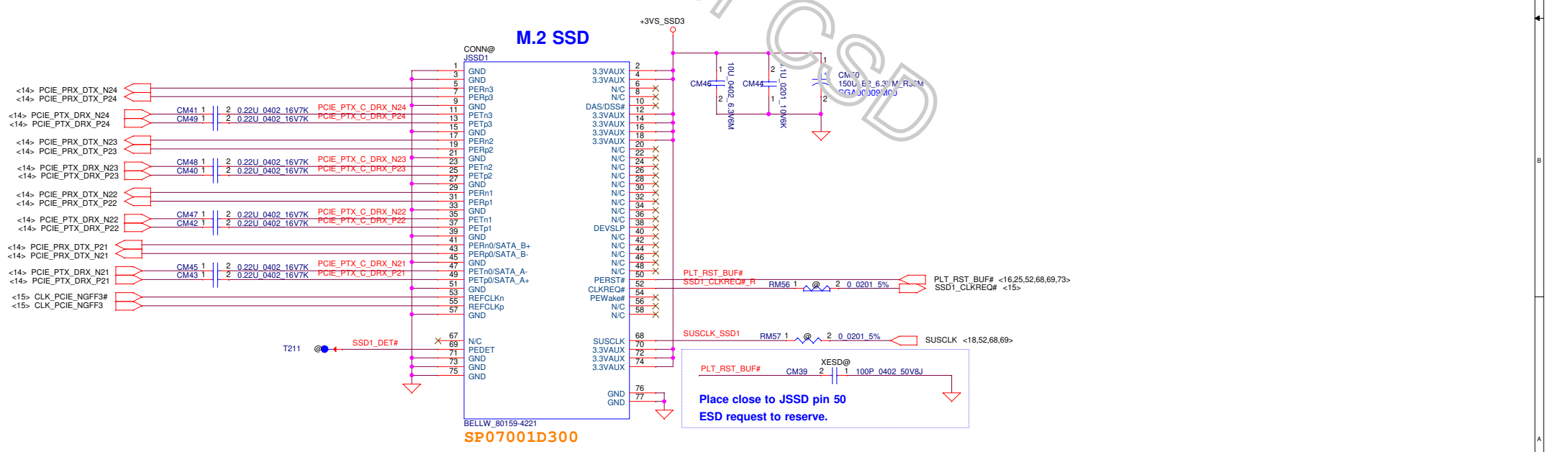
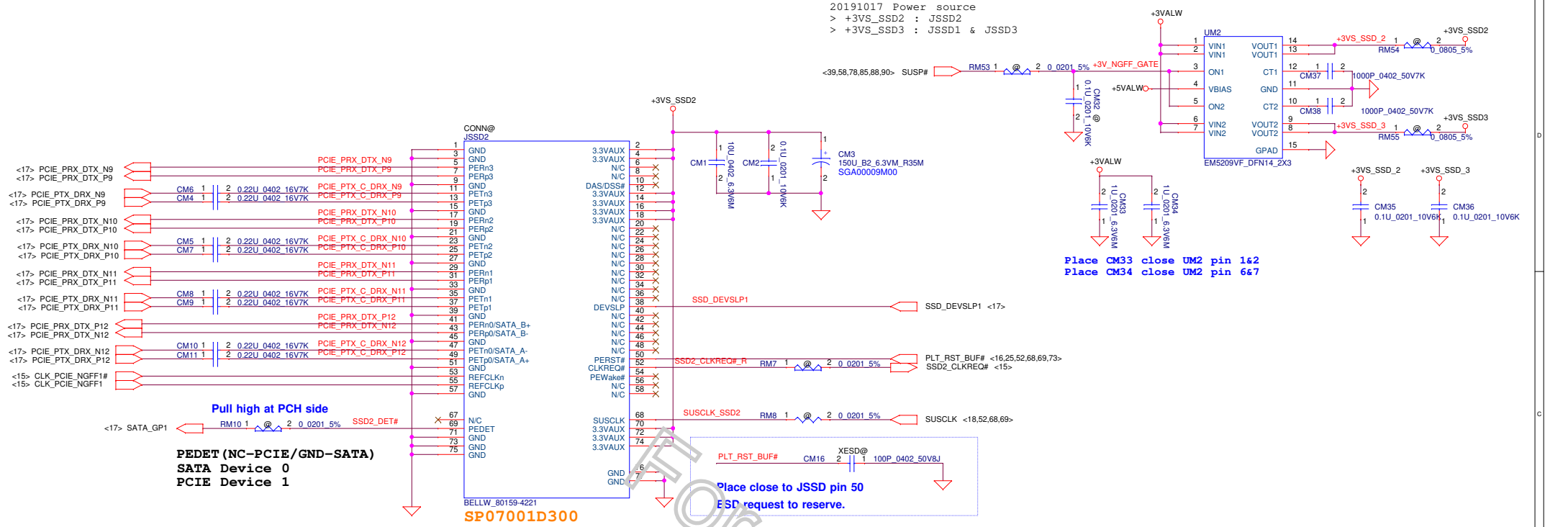


20190918

Remove HDD Re-driver

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2019/09/20		Deciphered Date		2020/09/20		Title	
										HDD/ Re-Driver/ G-sensor	
										Size Document Number	
										Rev	
										FH51M M/B LA-J871P	
										Date: Monday, March 02, 2020	
										Sheet 67 of 112	

20191017 Power source
> +3VS_SSD2 : JSSD2
> +3VS_SSD3 : JSSD1 & JSSD3

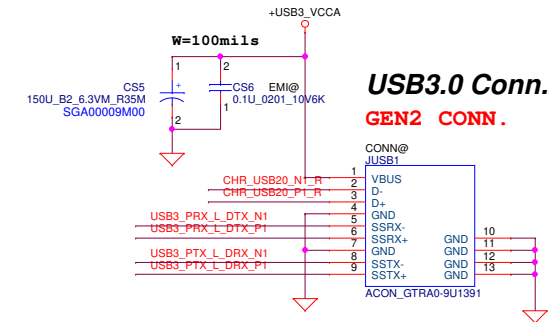
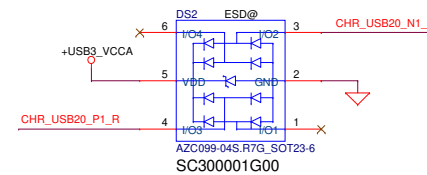
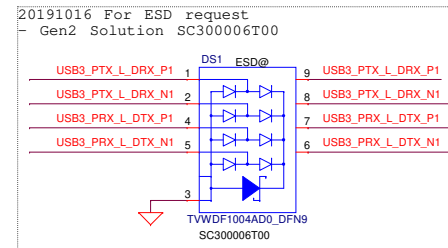
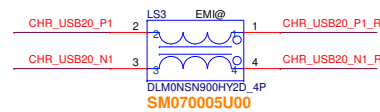
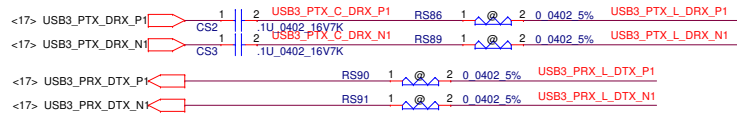


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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	
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Size	Document	Number	Rev	FH51M M/B LA-J871P	
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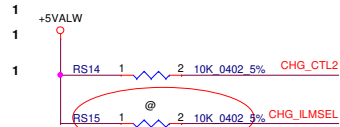
Reserve Page

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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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				Date: Monday, March 02, 2020	Sheet 70 of 112

USB3.0



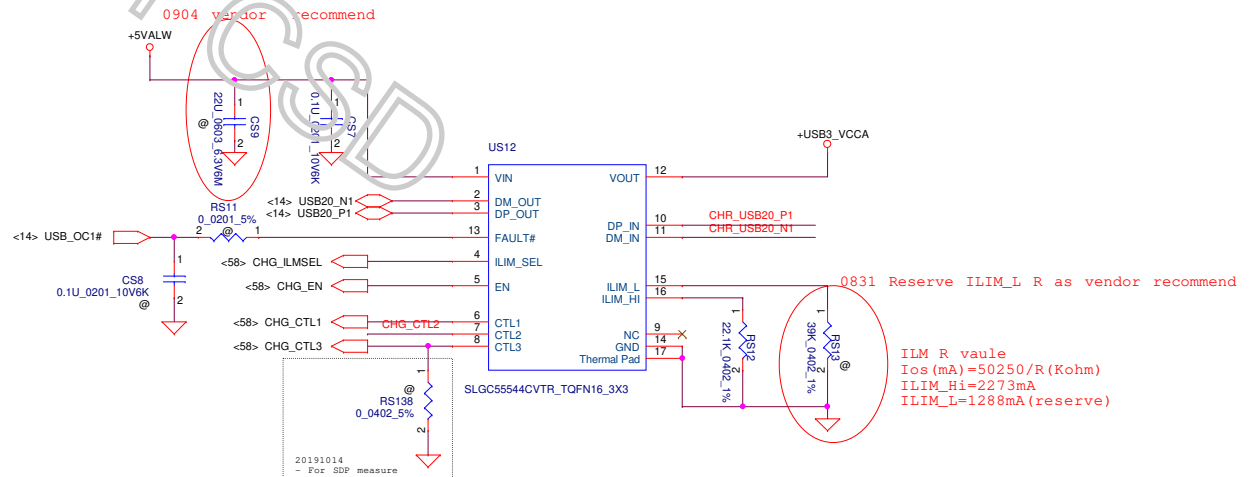
USB Host Charger



0911 Rerserve PU, vendor suggest to EC control
if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
	1	1	1	1	CDP	ILIM_H		Data Lines Connected



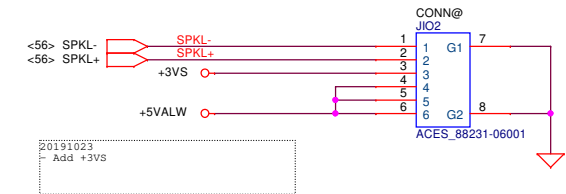
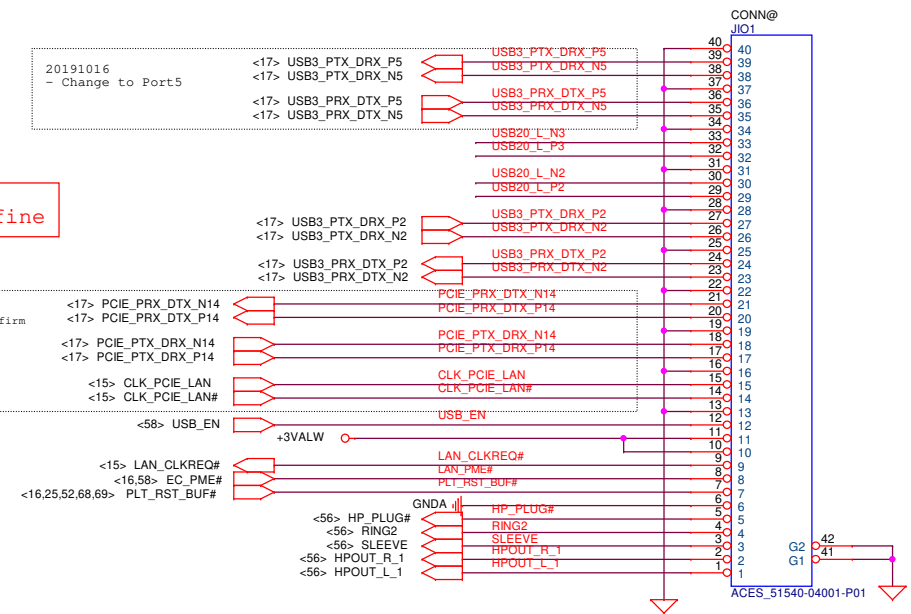
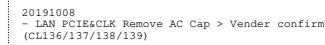
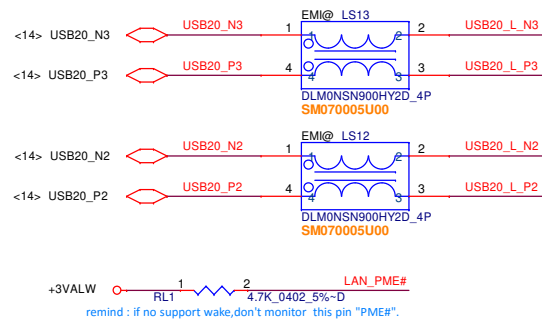
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title		
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				Size	Document Number	Rev
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20190918

USB3 Port3 move to IO/B

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IO/B CONN



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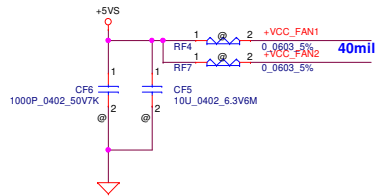
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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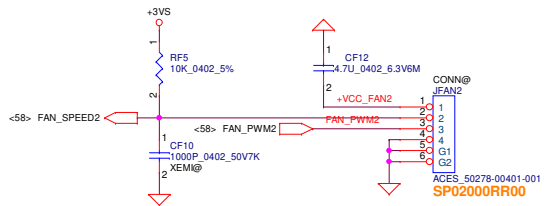
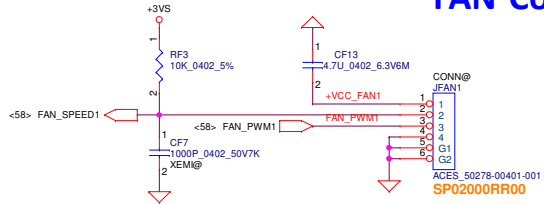
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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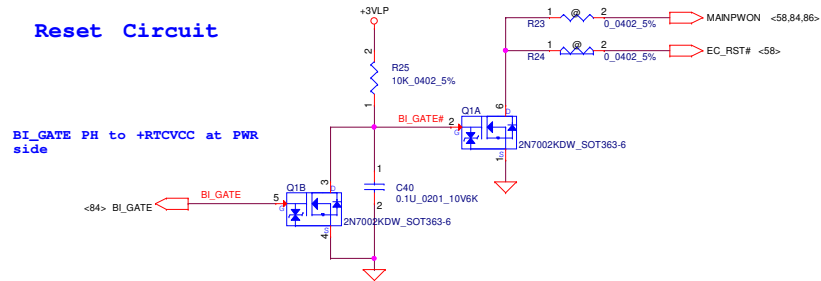
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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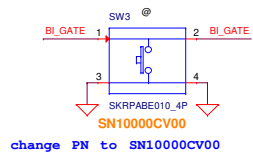
FAN Conn



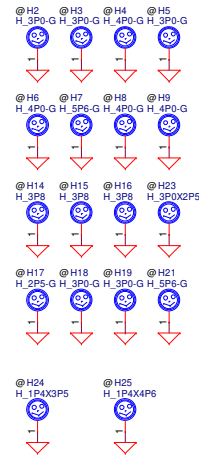
Reset Circuit



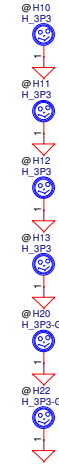
Reset Button



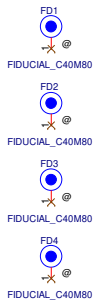
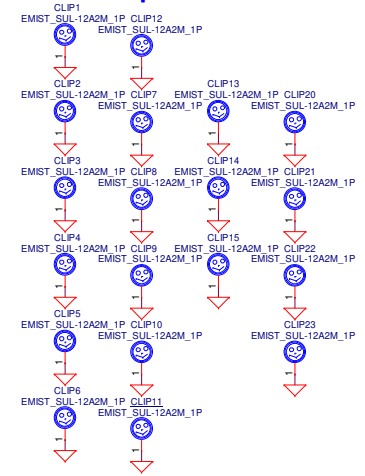
Screw Hole



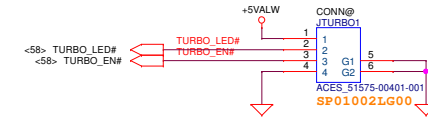
Stand Off



Clips

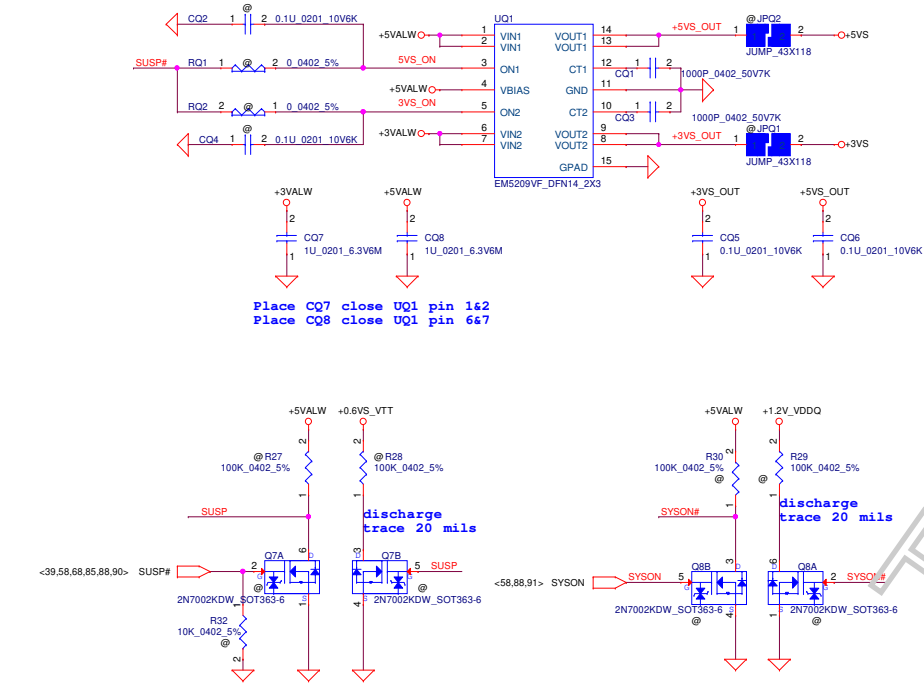


Turbo Key

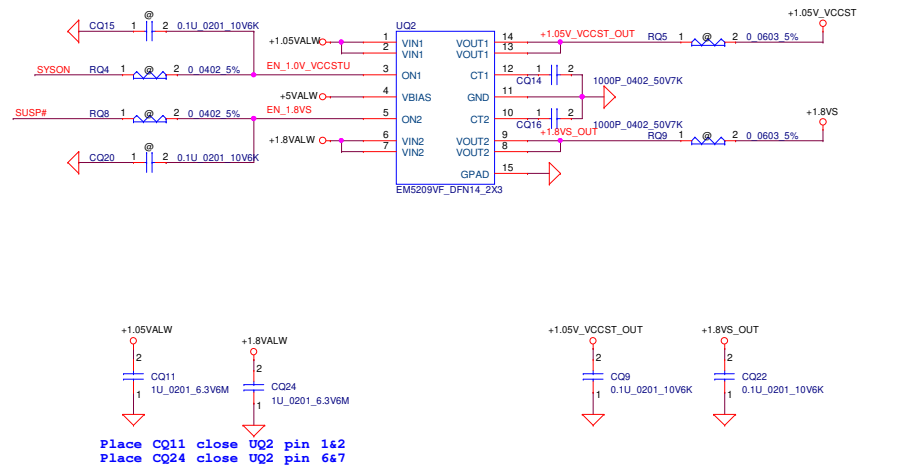


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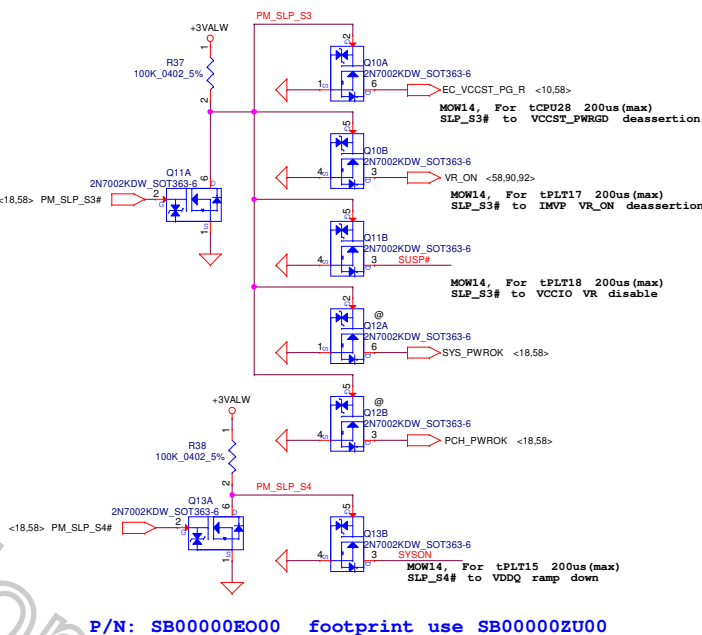
System DC interface



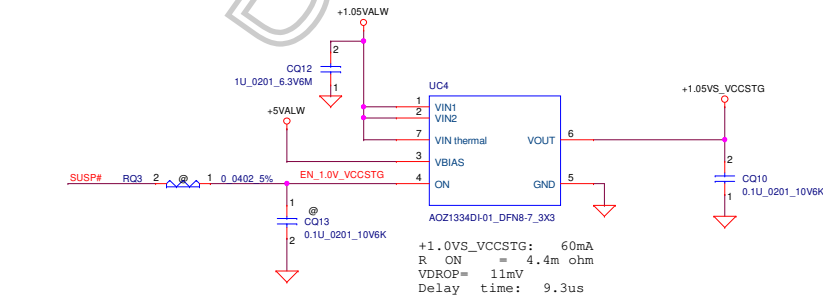
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



For Power ON/Off Sequence



+1.05VALW TO +1.05VS_VCCSTG



Reserve Page

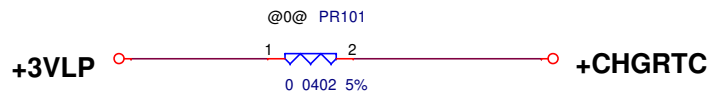
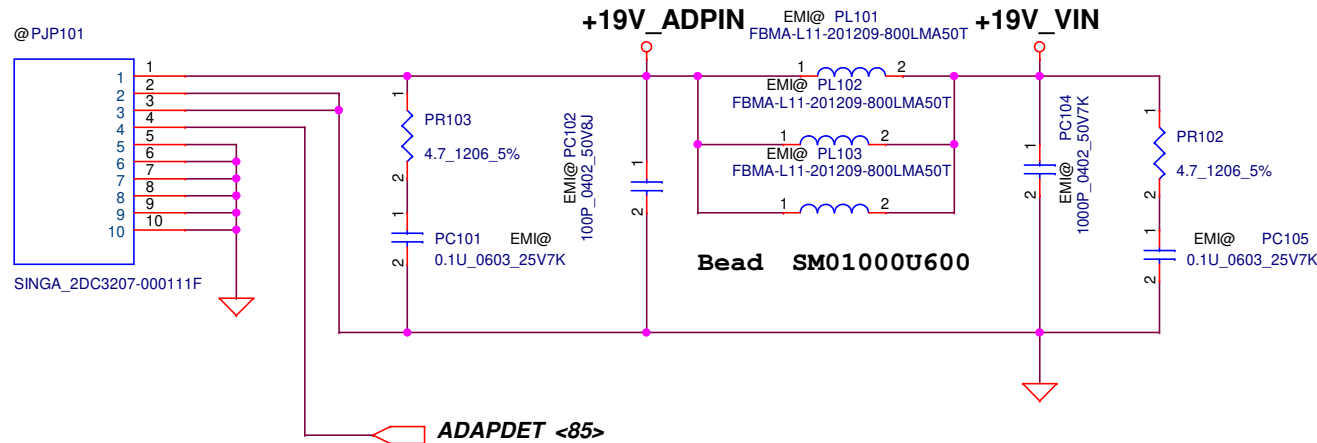
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18E-GDDR6 D
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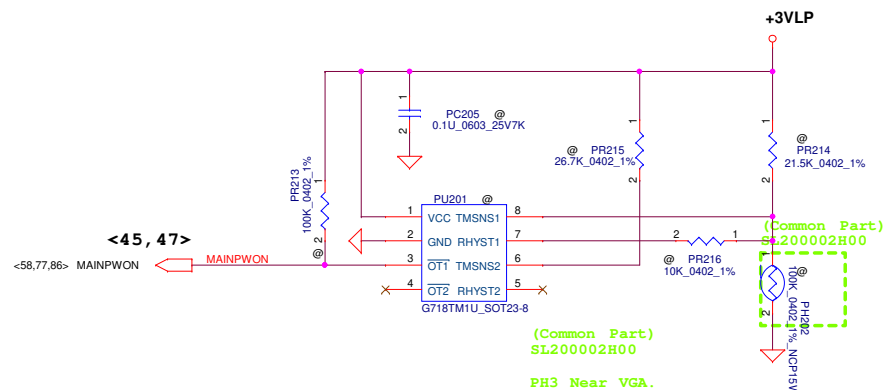
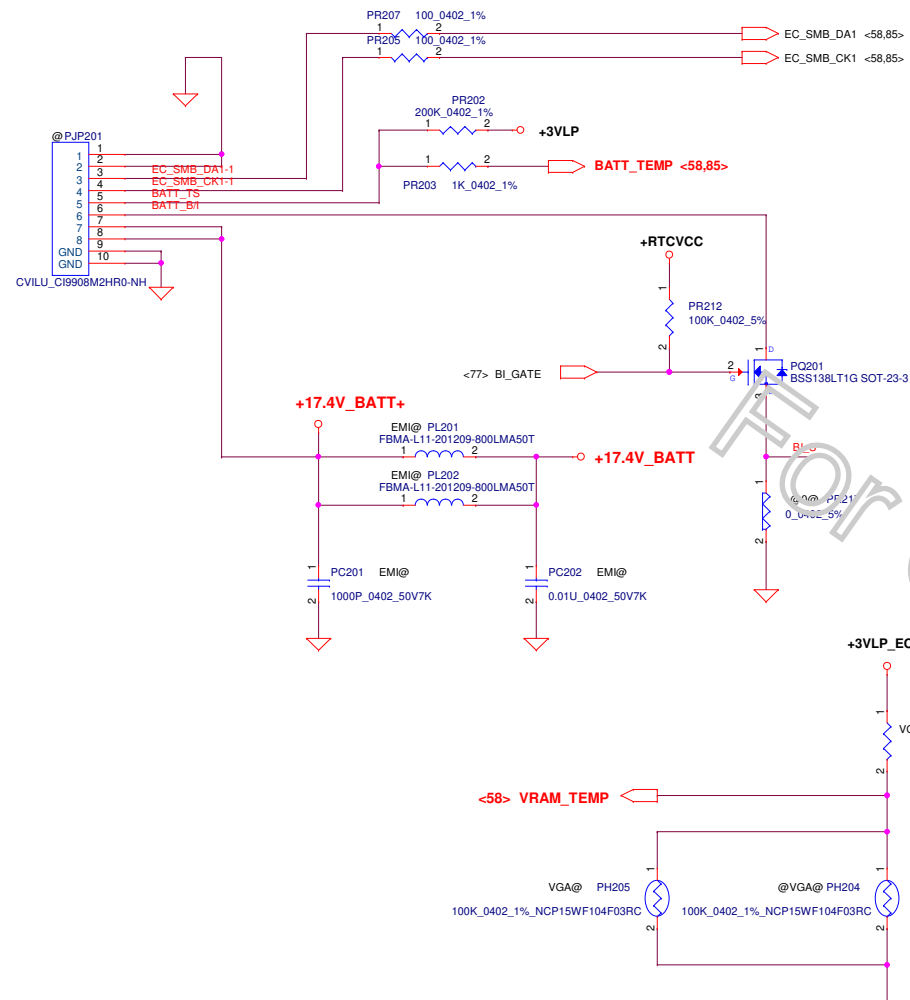
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Issued Date	2017/11/23	Deciphered Date	2017/12/31	Title					
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				1		83	of	112	
5		4		3		2		1	

Battery Bot Side

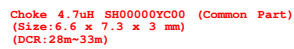
- PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



When PR204=18.7K

For OTP	KB9022	Active	Recovery
VCIN0_PH (V)	89'C, 1V	56'C, 2V	
PH202 (ohm)	8.0524K	26.11K	

$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$

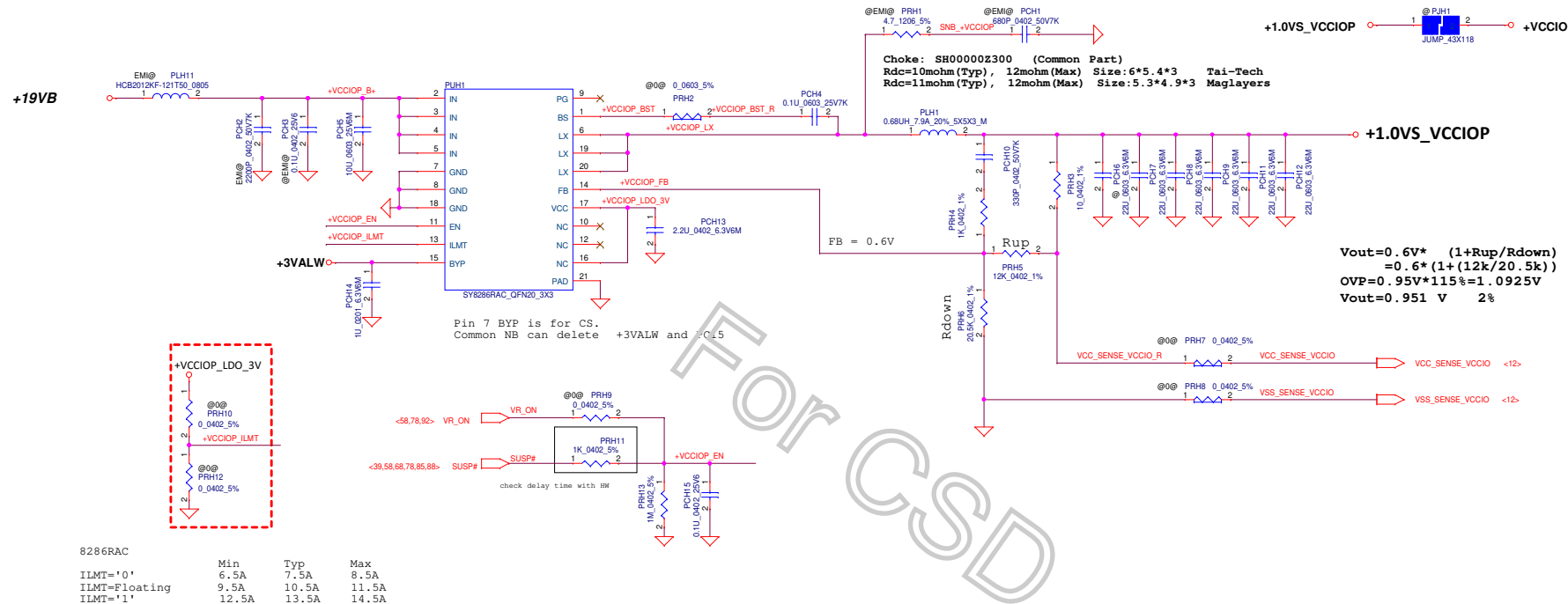


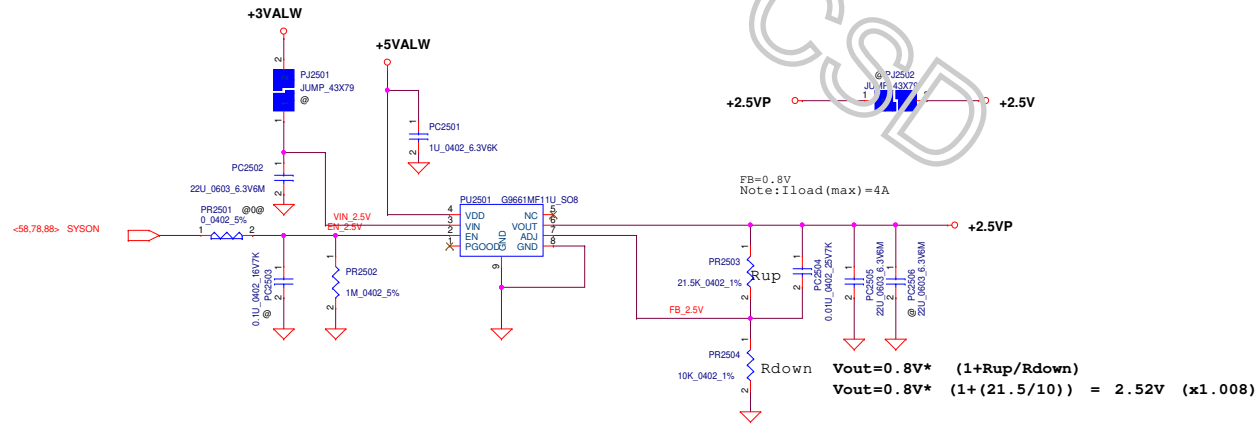
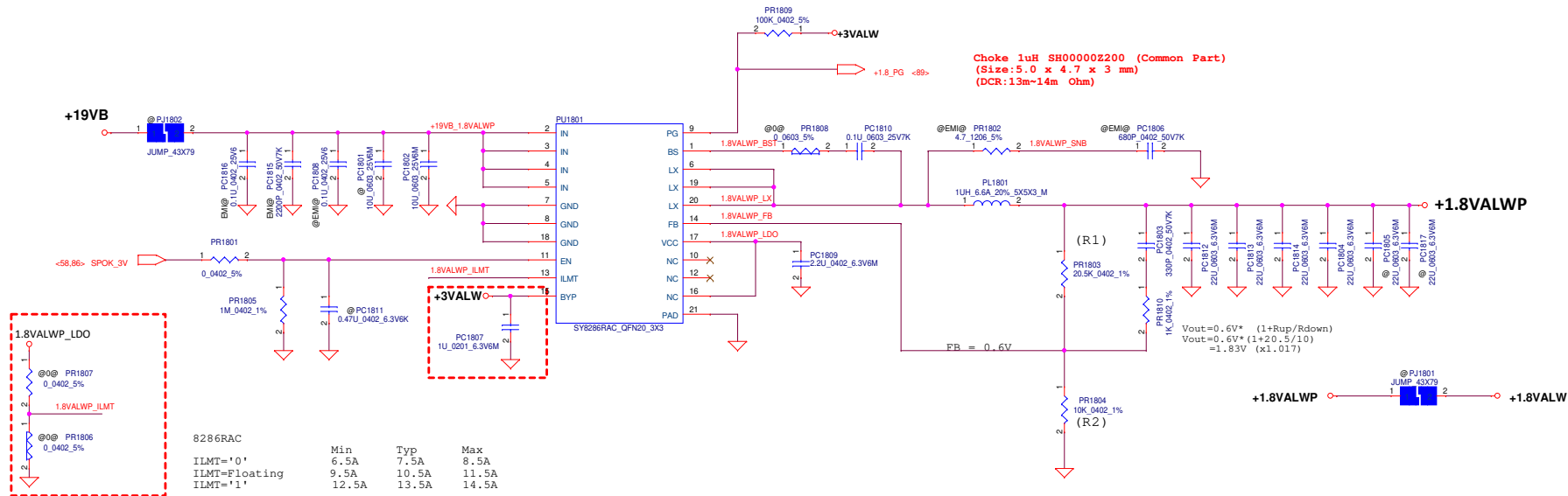
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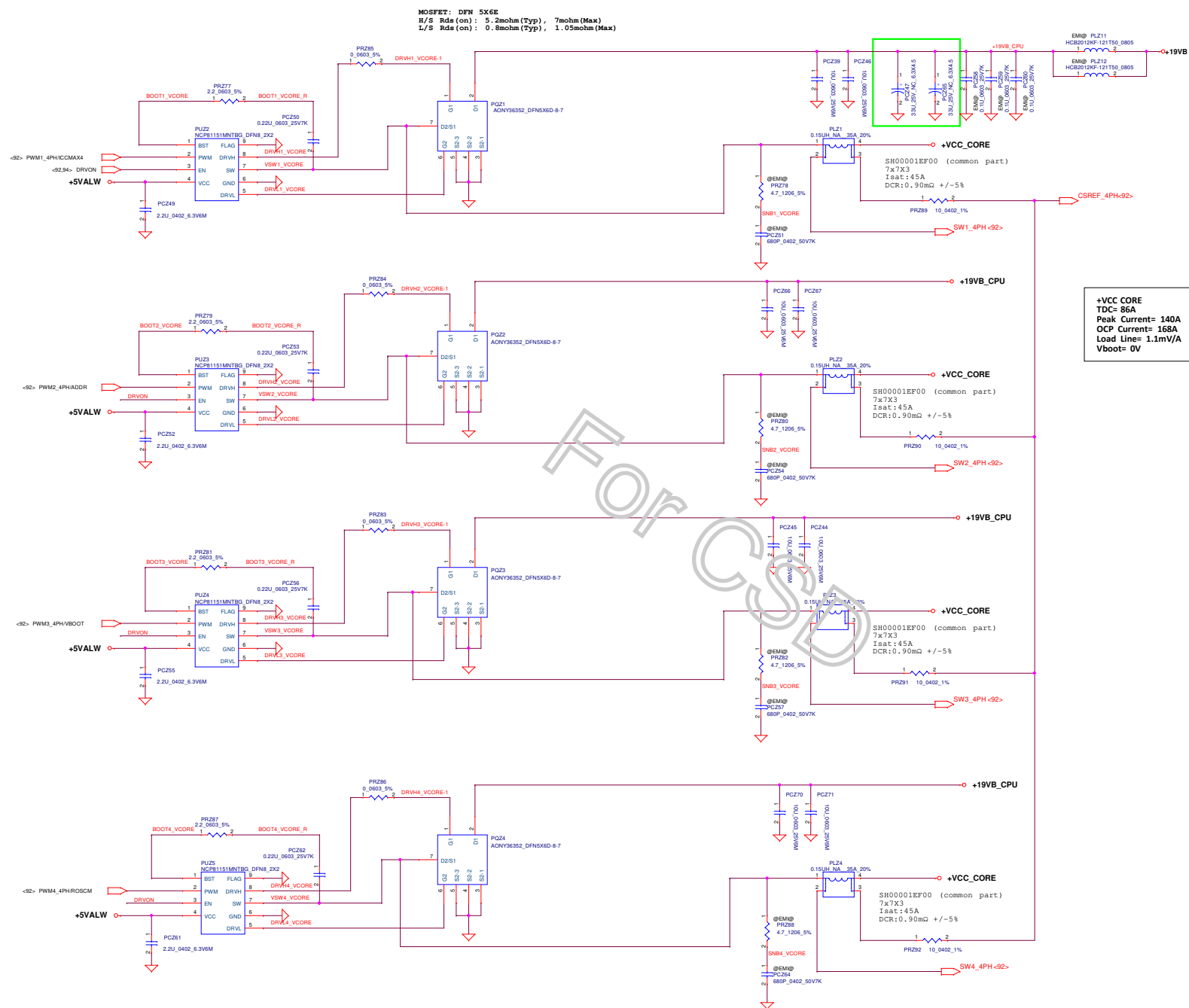
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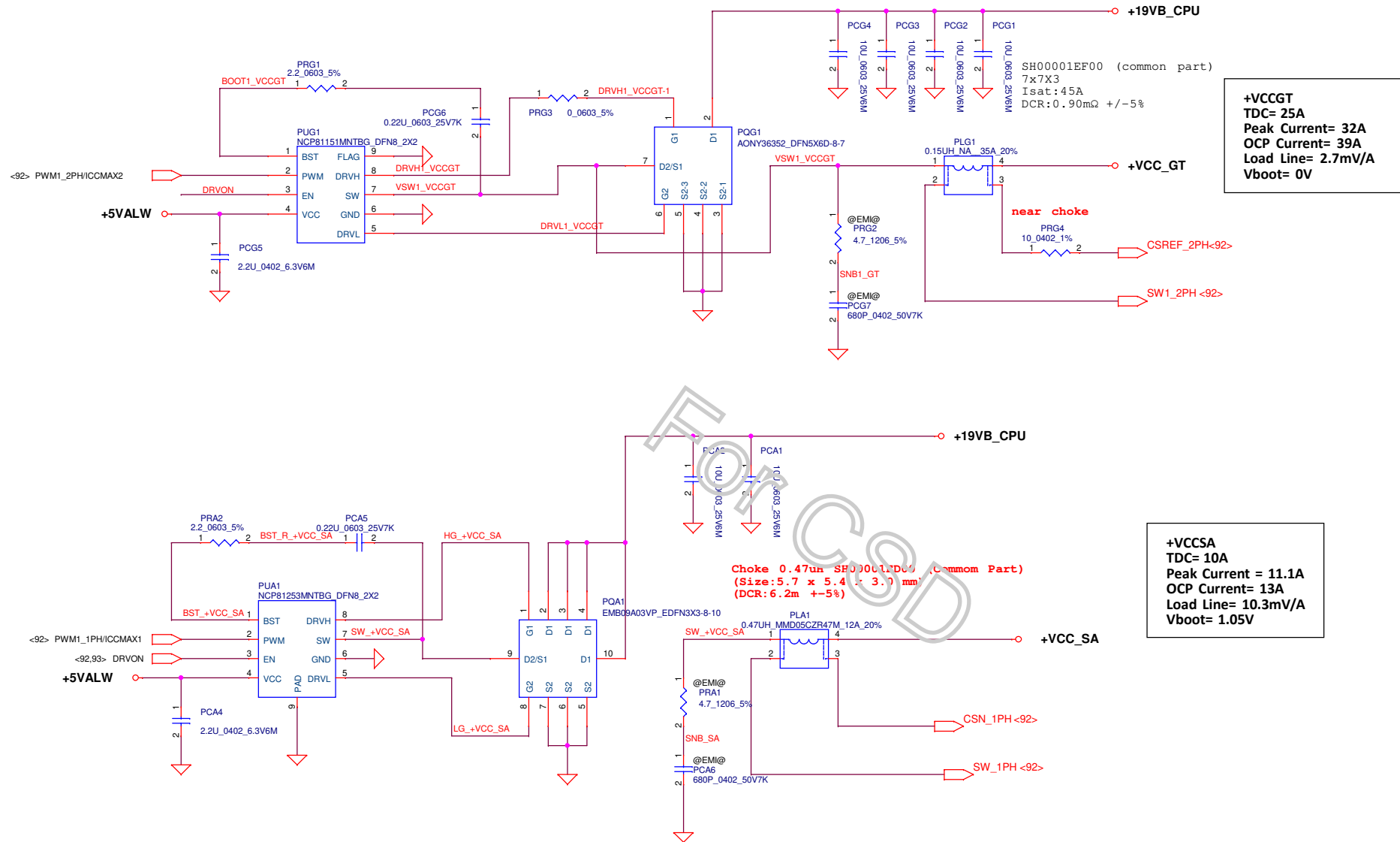




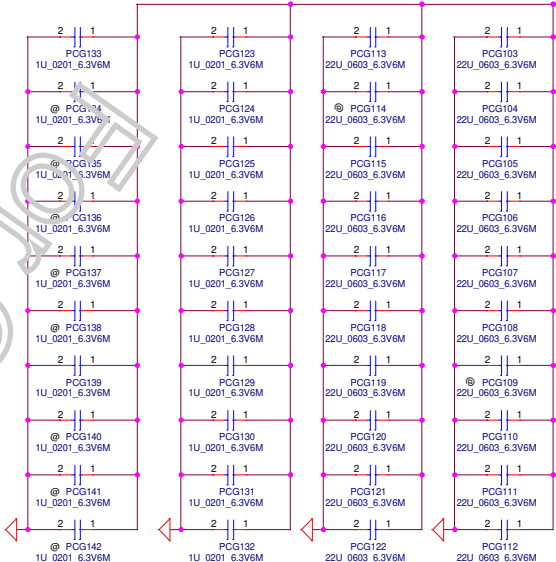
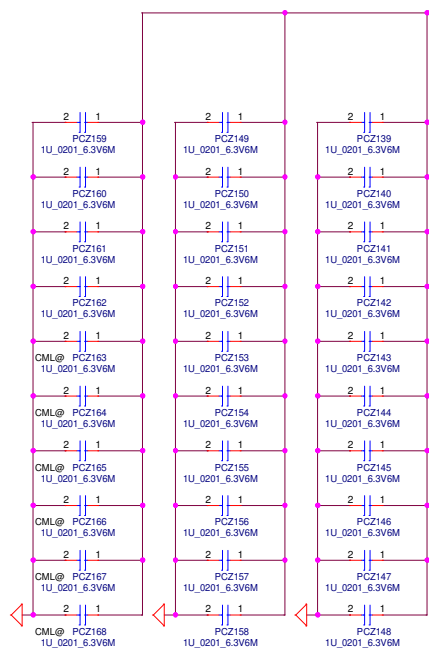
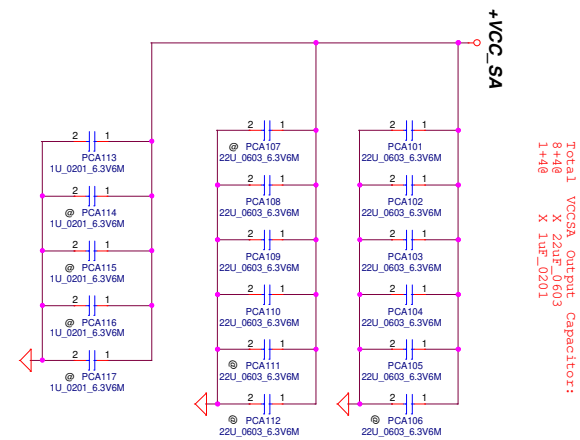
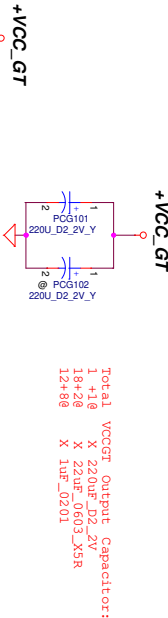
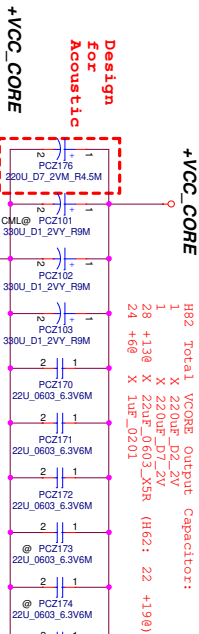


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Main Func = VCCGT/+VCCSA



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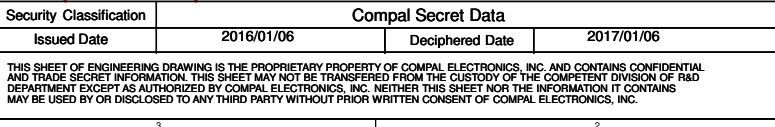
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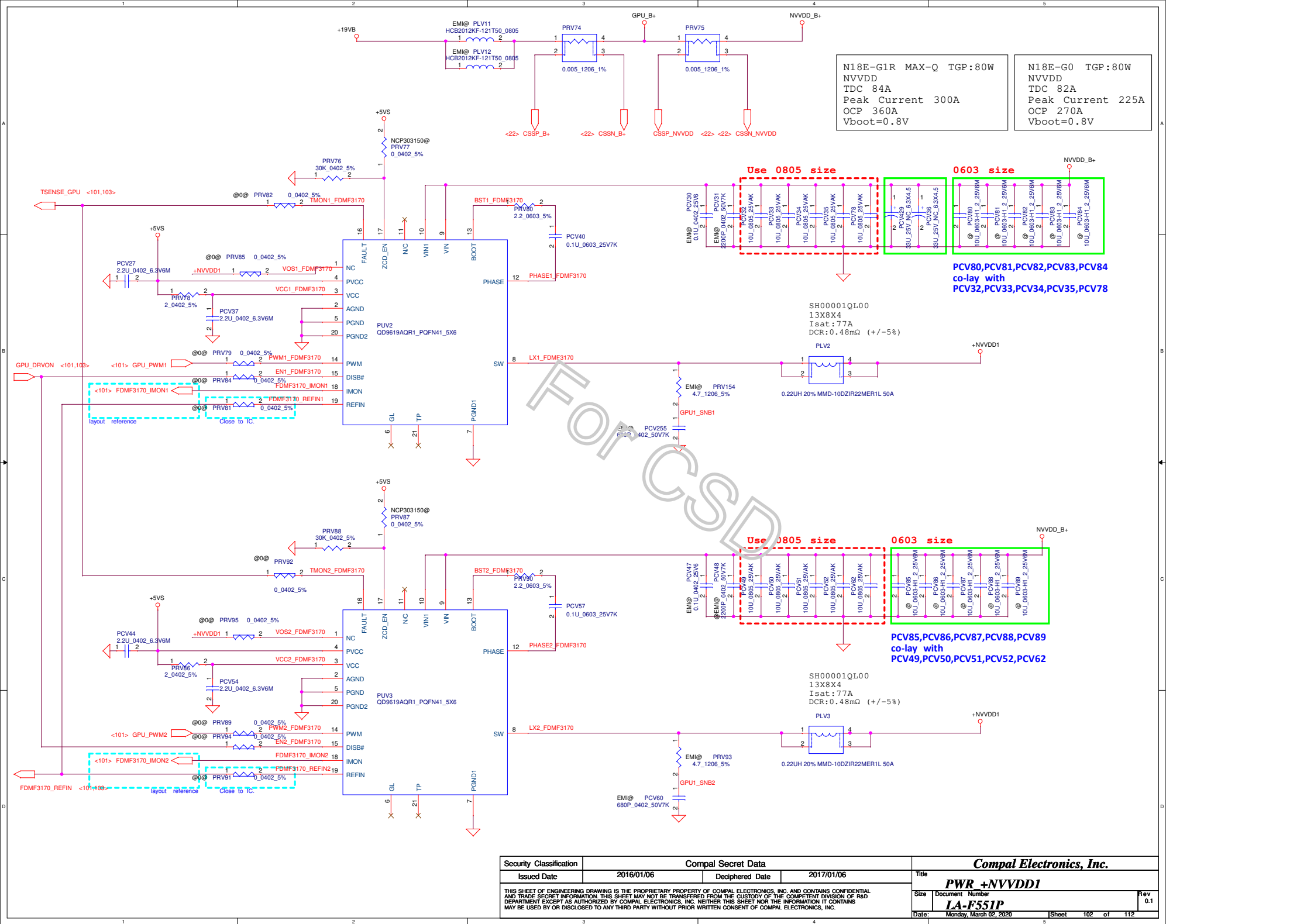
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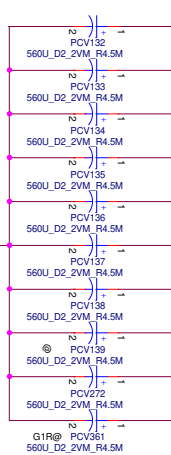
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+NVDD1
Place near GPU



Place under GPU

N18E-G1R MAX-Q TGP:80W
+NVDD
Imax:8.3A
560uF_D2_R4.5 X 10
22uF_0603 X 10 0X6
10uF_0402 X 23
1uF_0201 X 113 (93+20)

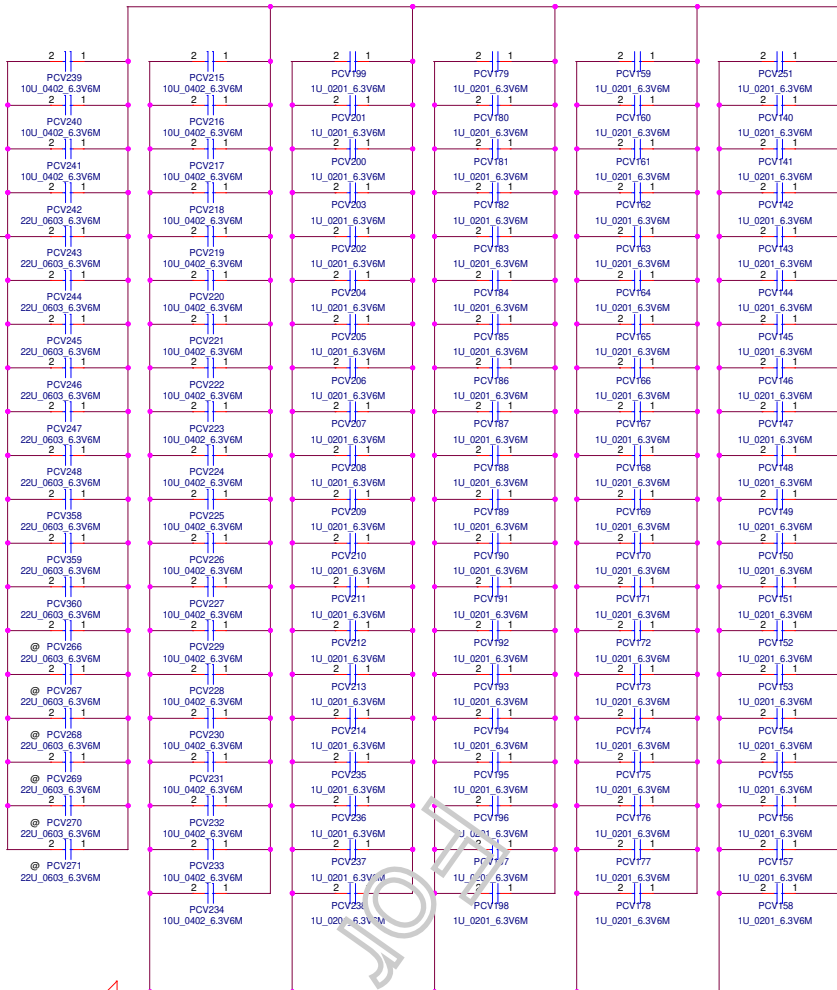
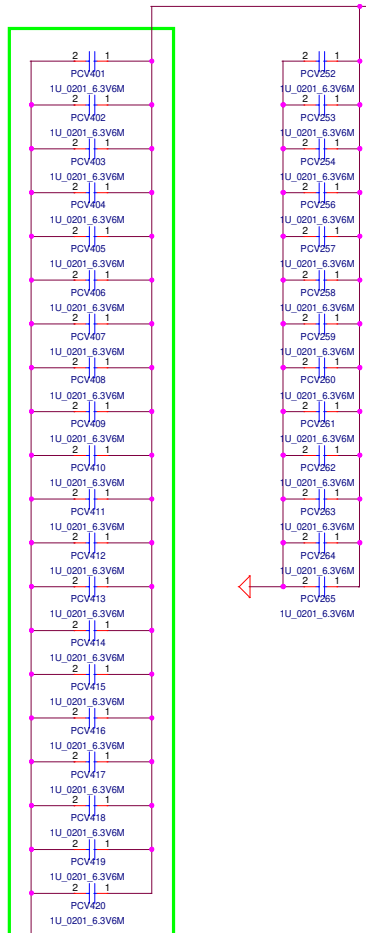


Table 5.10 GB48-256 Power Rail Filtering

Rail (GPU Rail) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB48-256 Package				
NVDD	Varies	(85 x 0.70U (0201W X65) 2 x 470uF (Pocap)		
		4 x 22uF (0603 X65)		
		3 x 47uF (0603 X65)		
		1 x 47uF (0603 X65)		



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Reserve VGA thermal sensor	0.1	84	Unpop PH205	11/12	A
02	Design Update	Reserve charger back to back mosfet for verify	0.1	85	Unpop PQB18,19	11/12	A
03	Design Update	Add 330uF for Coffee lake IA core output	0.1	95	Pop PCZ103	11/12	A
04	Design Update	Reserve 6 pcs of 22uF output cap for G1R-MaxQ sku	0.1	104	Unpop PCV266,PCV267,PCV268,PCV269,PCV270,PCV271	11/12	A
05	Design Update	shortage of SA0000AQE00 NCP81215MNTXG	0.1	92	change SA0000AQE00 to SA0000CTW00 NCP81215PMNTXG	11/12	A
06	Byer cost down action	PRB12 down size from 10ohm 1206 to 0805 size	0.2	85	PRB12 change from SD011100A80 to SD002100A80	12/10	B
07	X63ALYBOL01 change from "EG0,G1+CFL" to "EG1B+CML"	VCCORE Set to CML setting	0.2	92 95	1.PRZ47,PRZ50, PRZ52, PRZ54 change from SD014118380(118k) to SD014191380 (191k) 2.PRZ42 change from SD034301280(30.1k) to SD034187280 (18.7k) 3. Add PCZ101 (SE0000009S00) for CML 4. Add PCZ163,PCZ164,PCZ165,PCZ166,PCZ167,PCZ168(SE000000UC00) for CML	12/11	B
08	Design Update	Add PRB47,PRB48,PRB49 for reserving thermal sensing of B to B first MOSFET	0.2	85	Add PRB47,PRB48,PRB49 0 ohm (SD026000080)	12/11	B
09	Design Update	For VCCGT loadline tuning	0.2	92	PRZ49 change from SD034274380(274k) to SD034165380 (165k)	12/16	B
10	Design Update	For VCCSA IMON tuning	0.2	92	PRZ14 change from SD034280280(28k) to SD034294280(29.4k)	12/16	B
11	Design Update	Add 100k pull high 5VCC for disable VGA phase 4	0.2	101	Add PRV170 SD034100380 (100k)	12/09	B
12	Design Update	Setting right VRAM voltage for G1R and G1B GDDR	0.2	99	1.PRW25 change from SD034604280 (60.4k) to SD034374280 (37.4k) 2.PRW23 change from SD034787180 (7.87k) to SD034750180 (7.5k) 3.PRW24 change from SD034261280 (26.1k) and SD034187280(18.7k) to SD034249280(24.9k)	12/12	B
13	Byer cost down action	For lower cost	0.2	85	PCB18 change from SE00000WP00(2.2uF 25V) to SE000006S80 (2.2uF 16V)	12/09	B
14	Design Update	For optmial VCCCORE output cap	0.2	95	PCZ104,PCZ105,PCZ106,PCZ107,PCZ110,PCZ111,PCZ113,PCZ114,PCZ115,PCZ116,PCZ118,PCZ119,PCZ120,PCZ121,PCZ122,PCZ123,PCZ124,PCZ126,PCZ127,PCZ128,PCZ130,PCZ132,PCZ133,PCZ134,PCZ135,PCZ136,PCZ137,PCZ138,PCZ173,PCZ174 change to reserve	12/16	B
15	Byer cost down action	For lower cost	0.2	88	PCM6 change from SE000005T80 (10uF 0603) to SE00000M000 (22uF 0603) PCM7 change to reserve	12/09	B

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Version change list
(P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
16	Thermal issue	For decreasing frame buffer thermal over temp	1.0	84	Pop on PH205 unpop on PH204	1/2	C
17	Design update	Solution change	1.0	82 84	PR101 change from 0 ohm to r-short PR217 change from 0 ohm to r-short	1/7	C
18	Design update	Solution change	1.0	85 86	PRB15,PRB17,PRB23,PRB26,PRB8,PRB9 change from 0 ohm to r-short PR505 change from 0 ohm to r-short	1/7	C
19	Design update	Solution change	1.0	90 91	PRH7,PRH8 change from 0 ohm to r-short PR1806 change from 0 ohm to r-short	1/7	C
20	Design update	Solution change	1.0	92 99	PRZ9,PRZ11,PRZ12,PRZ27,PR72,PRZ73,PRZ25, PRZ18, PRZ30, PRZ32 change from 0 ohm to r-short PRW26,PRW14,PRW20,PRW9 change from 0 ohm to r-short	1/8	C
21	Design update	Solution change	1.0	101	PRV20,PRV34,PRV50,PRV70,PRV12,PRV13,PRV16,PRV18,PRV145,PRV146,PRV147,PRV54,PRV56,PRV58 change from 0 ohm to r-short	1/8	C
22	Design update	Solution change	1.0	102	PRV82,PRV85,PRV79,PRV84,PRV81,PRV92,PRV95,PRV89,PRV94,PRV91,PRV102,PRV105,PRV99, PRV104,PRV101 change from 0 ohm to r-short	1/8	C
23	Design update	For VCCCORE transient tuning	1.0	95	Pop on PCZ119,PCZ120	2/5	C

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92		11/14	A
02	Design Update	solution change	83, 85 90, 91		11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91		11/16	A
04	Design Update	For CPU transient	89, 92		11/19	A
05	Design Update	solution change	84		12/3	A
06	Design Update	solution change	87		12/12	B
07	Design Update	solution change	83, 97		12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 鋁 皮 離 ESD 能量透過 HS 小板及 HS cable coupling 到板造成 打	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE000006880) for EMI request	1/15	B
11	Design Update	Design change	90, 87	delete boost circuit and PCZ47	5/7	FH58F EVT
12	Design Update	Design change	90, 87	delete PC1112	5/7	FH58F EVT
13	Design Update	Design change	88, 93	change PCB15 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to 1U 16V K X5R 0402(SE000000OU00) change PCB16 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to S CER CAP 2.2U 16V K X5R 0402(SE000013780) Add PLV2, PLV3 second source S COIL .22UH TMPC1004H-R22MG-R5505-D 50A(SH00001XH00)	6/25	INV2
14	Design Update	change CH_OC to 75A	95	change PRV71 from S RES 1/16W 133K +-1% 0402(SD034133380) to S RES 1/16W 113K +-1% 0402(SD034113380)	6/25	FH58F PVT

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	52	CNVi	1209	CNVi-Intel review (FH5VF)	Add RM67 / RM68 0-ohm Add PU RM70 / PD RM69 (Reserve)		
2	52	UART_BT	1209	UART_BT review	RM66 Change to @ for Vender review		
3	17/69	JSSD3	1209	JSSD3 SATA/PCIE detect	SATA6P change to 6P4 & RH303 PU		
4	64	EMR	1209	EMR Power source	RH285/RH286/RH292 power source change to +3VALW		
5	19	PROJECT ID	1209	PROJECT ID	defined as Project - 60 (ID1:H / ID0:H)		
6	38	Panel OD	1209	Panel OD function	RX11 change to unpop & BIOS needs to detect panel to select H or L .		
7	16/58	BT_ON	1209	BT_ON change to PCH	RH304 pop (PCH) & RB85 unpop (EC)		
8	15/68/69	M.2 SSD	1209	Fixed naming	> SSD1 - GPP_B9/CLKREQ4# (PCIE only) (2018 @SSD2) > SSD2 - GPP_B8/CLKREQ3# (PCIE/SATA) (2018 @SSB1) > SSD3 - GPP_B10/CLKREQ5# (PCIE/SATA) (2019 NEW) > PEDET naming		
9	52	CNVi	1209	CNVi-Intel review (FH5VF)	RM70 change power source to +3VS_WLAN		
10	58	Board ID	1209	Board ID config	ADD DVT@ & DVTR6B@ for DVT BOM		
11	18/23/58/63	DRAM/SYSON/TP	1209	ESD	> Add CH55 33p & EDS@ > Change CD10 to XESD@ > Change CB12/CB13 to 33p & ESD@ > Add CK203 680p & ESD@		
12	58	EC	1209	EC_SMB_CK3/DA3	> RB79/RB80 change power source to +5VS		
13	81-111	PWR SCH	1209	POWER update	Combined Power SCH (1209A)		
14	77	Screw Hole	1210	DDR Shielding	> Add CLIP11		
15	81-111	PWR SCH	1210	POWER update	Combined Power SCH (1210A)		
16	81-111	PWR SCH	1210A	POWER update	Combined Power SCH (1210B)		
17	52	CNVi	1211	CNVi-Intel review (FH51M)	> RM69 change to 71.5k & CNVi@ > RM70 set CNVi@ > RH22 change to 20K > RM36/RM37/RM67/RM68 change to 22 ohm		
18	73	IO_B conn.	1211	IO_B conn.	> Change IO_B pin definition		
19	69	SSD3	1211	BOM Config	> ADD "SSD3@" for BOM		
20	81-111	PWR SCH	1213	POWER update	Combined Power SCH (1213)		
1	20/3842/56	PCH/eBP/Type-C/Audio	0113	BOM Config / Short pad	> Change RH100/RS137/RA9 to short pad > Change RX8/RX9/RA14 BOM structure to EMI@		
2	81-111	PWR SCH	0113	POWER update	Combined Power SCH (0113)		
3	81-112	PWR SCH	0115	POWER update	Combined Power SCH (0115)		
4	16	PCH	0115A	ROM co-lay	> Delete JC1 for co-lay		
5	81-113	PWR SCH	0116	POWER update	Combined Power SCH (0115B)		

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